

Integration of Reconfigurable Hardware into the DETER Testbed

John W. Lockwood
lockwood@arl.wustl.edu

<http://www.arl.wustl.edu/~lockwood/>

Todd Sproull
todd@arl.wustl.edu



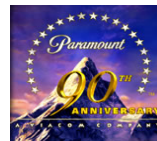
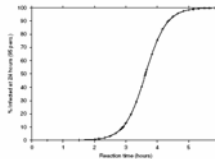
Applied Research Laboratory: Reconfigurable Network Group
<http://www.arl.wustl.edu/projects/fpx/reconfig.htm>

Outline

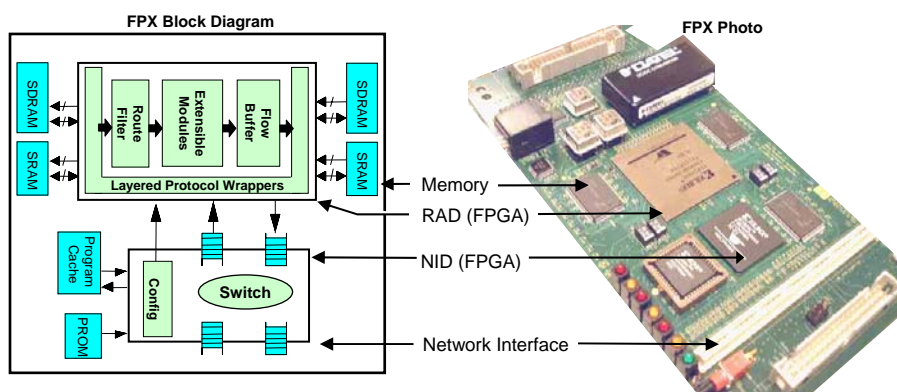
- **Motivations for hardened networks**
 - Wire-speed processing with the Field Programmable Port Extender (FPX) Platform
- **Systems using the FPX Platform**
 - Global Velocity GVS-1000 Rackmount Chassis
 - Washington University Gigabit Switch
- **Comparison to other FPGA-based Platforms**
 - NetFPGA2 (Stanford)
 - BEE2/RAMP (Berkeley)
- **Application Development**
 - Design Flow
 - Testbed Integration
- **Objectives for integration with DETER**

Interested Parties for Hardened Networks

- **Who cares about computer virus attacks**
 - Network users
 - Universities
 - Government
- **Who cares about copyright**
 - Record Companies and Movie Studios
 - Entertainers, Authors
- **Who cares about confidential data**
 - Business with proprietary information
 - Health care, Government,
 - Individuals with proprietary information
- **Who cares about infrastructure**
 - Network operators
 - Industry
 - Government

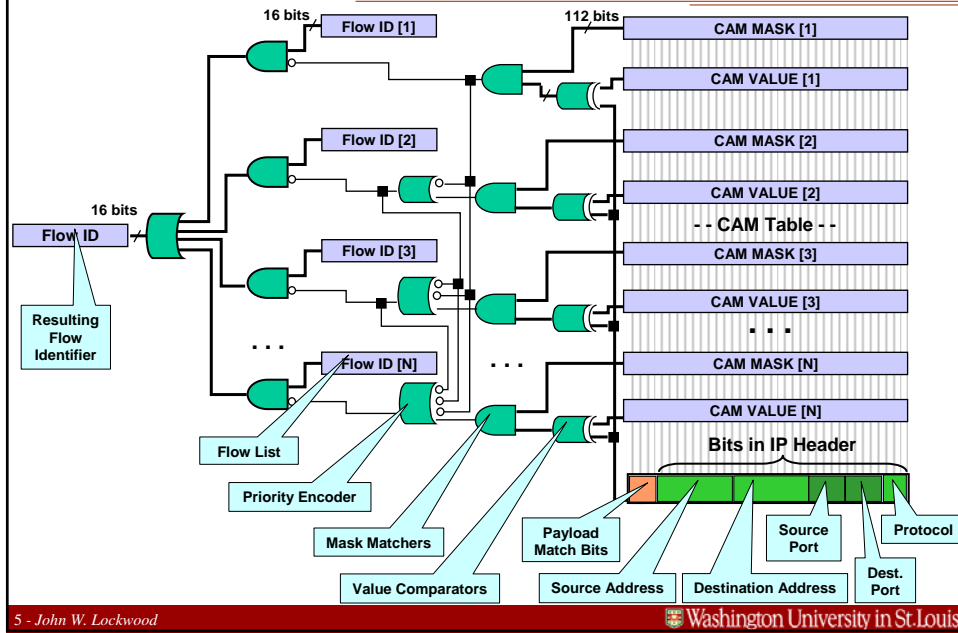


Field Programmable Port Extender (FPX)

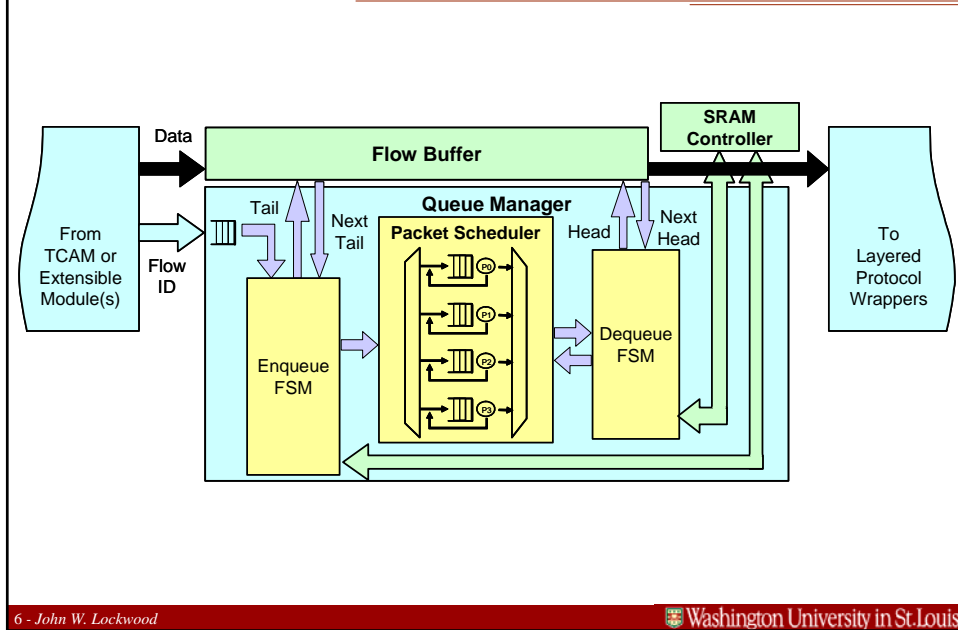


**Wire-speed Network Processing
using Reconfigurable Hardware**

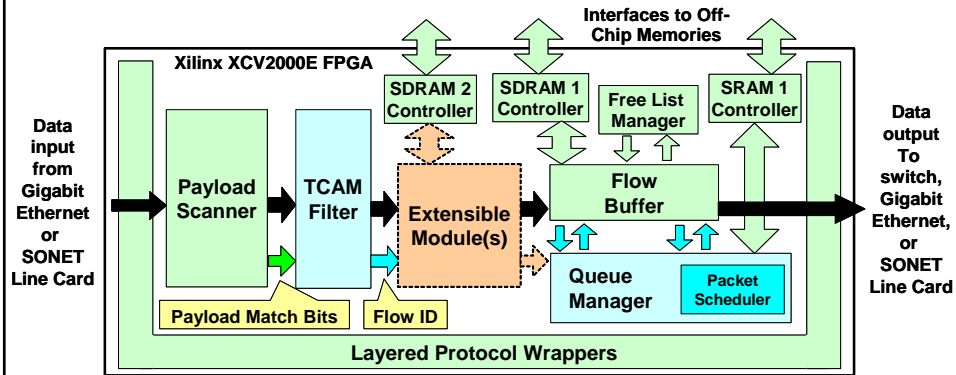
TCAM Packet Classifier on the FPX



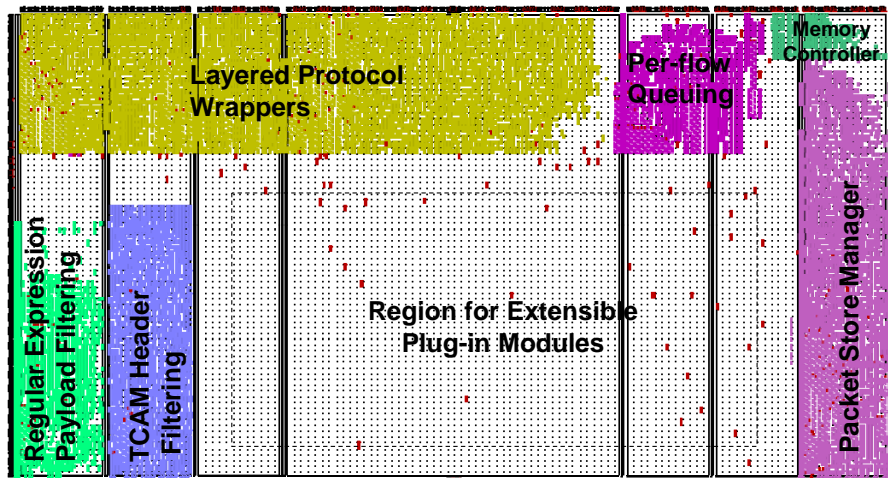
Per-flow Queue Management on the FPX



System-On-Reprogrammable Chip



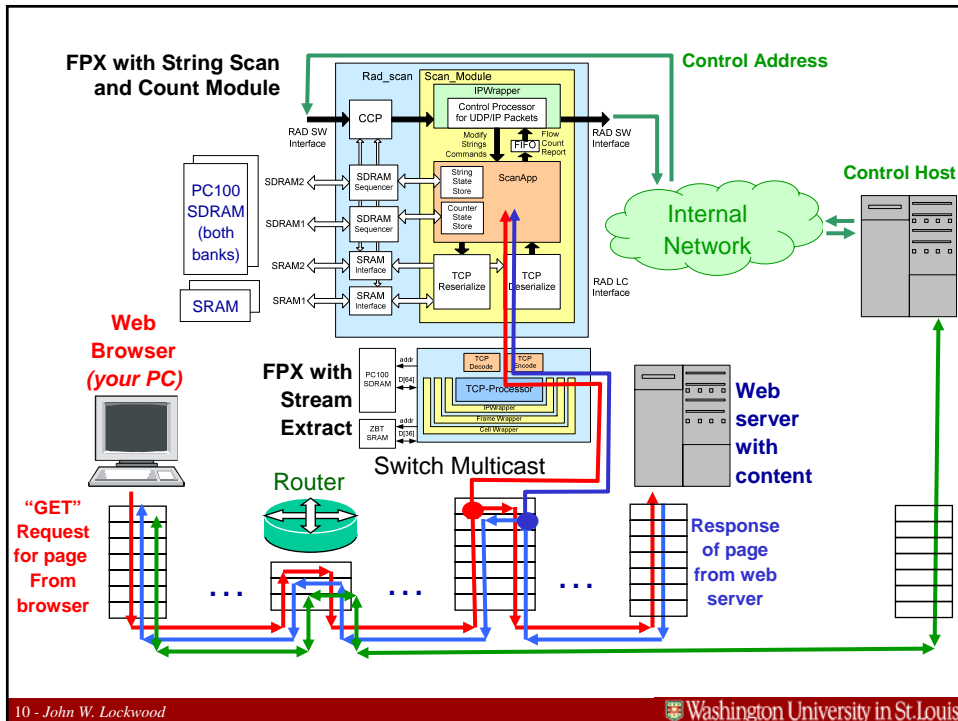
Firewall / IDP: FPGA Layout on FPX Platform



FPGA Layout of SOC Firewall / IDP on Virtex 2000E, as mapped to FPX Platform

Modules Implemented on the FPX

- **Intrusion Detection and Prevention**
- **IPv4 CAM Filter**
 - 104 Bit header matching
- **IPv6 Tunneling Module**
 - Tunnels IPv6 over IPv4
- **Traffic Generator**
 - Per-flow mixing
- **Video Recoder**
 - Motion JPEG
- **Hardware/Software Processing**
 - PicoBlaze
 - LEON2
- **EarlyBird Worm Detection**
- **Statistics Module**
 - Detailed Event counters
- **Fast IP Lookup (FIPL)**
 - Longest Prefix Match
- **Packet Content Scanner**
 - Reg. Expression Search
- **Data Queuing**
 - Per-flow queue in SDRAM



```

22:25:40.439353 agent-jones.arl.wustl.edu.http > armadillo182.cse.wustl.edu.3914:
  F 854:854(0) ack 473 win 6432 (DF)
0x0000 4500 0028 13a5 4000 4006 e551 80fc 992a      E..(..@..Q...*
0x0010 80fc a6b6 0050 0f4a 10b9 31e7 7346 508b      .....P.J..l.sFP.
0x0020 5011 1920 3ece 0000                                P...>...

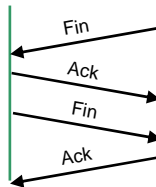
22:25:40.444977 armadillo182.cse.wustl.edu.3914 > agent-jones.arl.wustl.edu.http:
  . ack 855 win 16667 (DF)
0x0000 4500 0028 9365 4000 7f06 2691 80fc a6b6      E..(.e@...&....
0x0010 80fc 992a 0f4a 0050 7346 508b 10b9 31e8      ...*.J.PsFP...l.
0x0020 5010 411b 16d3 0000 0000 0000 0000      P.A.....

22:25:40.446736 armadillo182.cse.wustl.edu.3914 > agent-jones.arl.wustl.edu.http:
  F 473:473(0) ack 855 win 16667 (DF)
0x0000 4500 0028 9366 4000 7f06 2690 80fc a6b6      E..(.f@...&....
0x0010 80fc 992a 0f4a 0050 7346 508b 10b9 31e8      ...*.J.PsFP...l.
0x0020 5011 411b 16d2 0000 0000 0000 0000      P.A.....

22:25:40.446745 agent-jones.arl.wustl.edu.http > armadillo182.cse.wustl.edu.3914:
  . ack 474 win 6432 (DF)
0x0000 4500 0028 13a6 4000 4006 e550 80fc 992a      E..(..@..P...*
0x0010 80fc a6b6 0050 0f4a 10b9 31e8 7346 508c      .....P.J..l.sFP.
0x0020 5010 1920 3ecd 0000                                P...>...

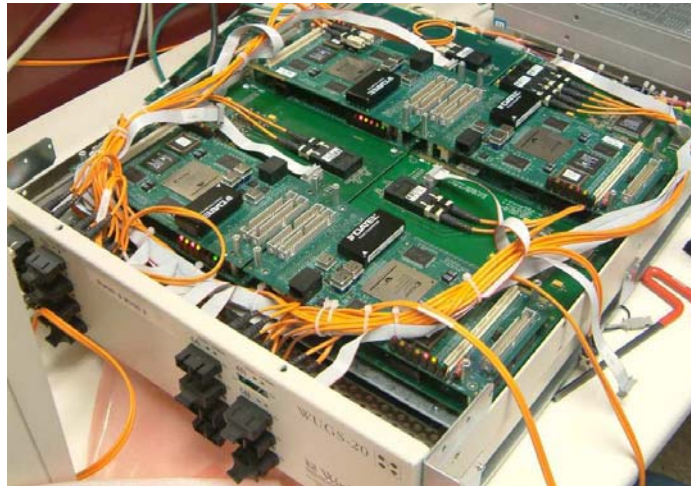
```

End Host: Windows XP
with Internet Explorer
armadillo182.cse.wustl.edu



Web server : Apache
agent-jones.arl.wustl.edu

WashU Gigabit Switch with FPX Modules



3-U Rackmount Chassis with
8 Gigabit Ethernet Ports

Global Velocity Chassis with FPX Hardware



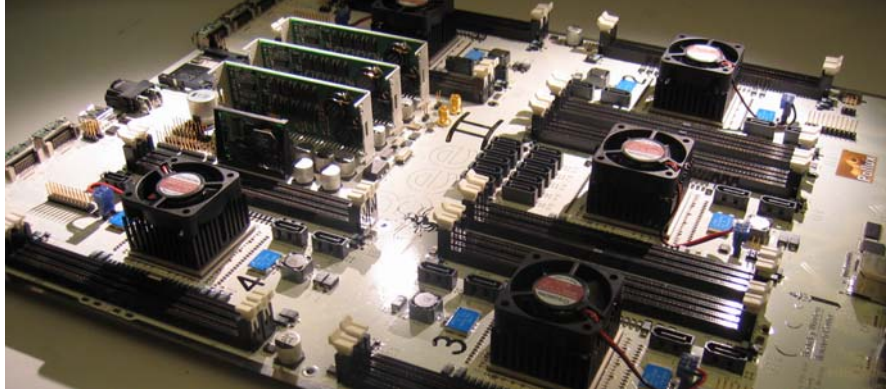
**3-U Rackmount Chassis with
up to 8 stacked FPX Modules**

Stanford's NetFPGA2



- Applications developed for FPX could be ported to NetFPGA2
- Each NetFPGA2 board supports 4 Gigabit Ethernet Ports
- Each FPX board supports 2 OC-48 or Gigabit Ethernet ports
- NetFPGA's V2Pro30 faster than FPX's V2000E
- NetFPGA's V2Pro30 smaller than FPX's V2000E

Berkeley's BEE2 / RAMP Platform



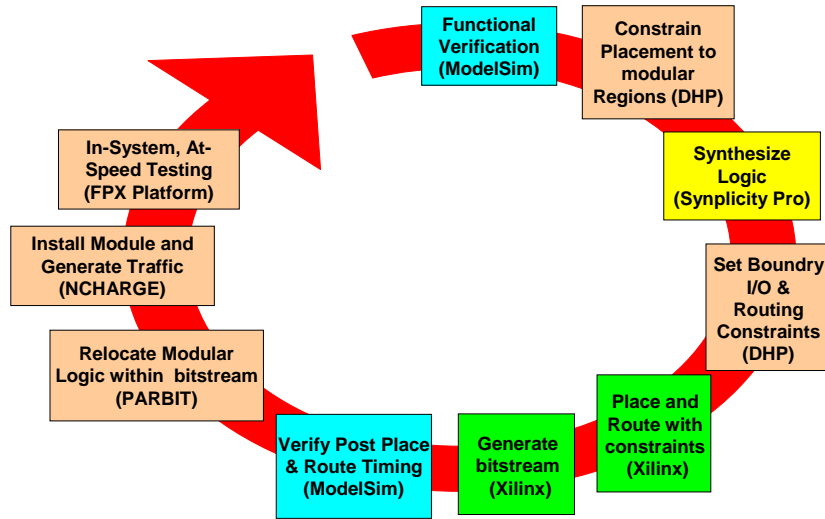
- BEE2 optimized for DSP rather than Internet Packet Processing
- FPX Packet processing Applications could be ported to BEE2
- BEE2 has more FPGA and DRAM resources than FPX
- FPX has OC48 and Gigabit Ethernet Ports
- BEE2 could support 10 Gigabit link interfaces (using four bundled 3.125 Gbps channels / port)

GVS-1000 Chassis with Gigabit Ethernet



**3-U Rackmount GVS-1000 Chassis with
FPX Modules and 2 Gigabit Ethernet Interfaces**

Reconfigurable Hardware Design Flow



FPX used for Hands-on Tutorials

Gigabit Kits workshops with FPX Tutorials



Participants Programmed FPX Modules in the CAD Laboratory

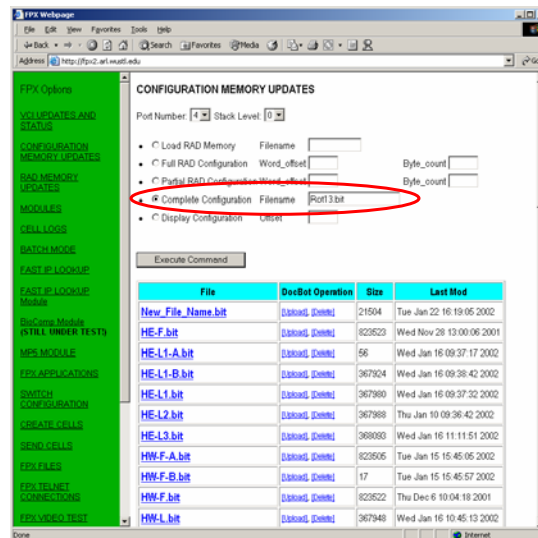


Then tested modules in lab



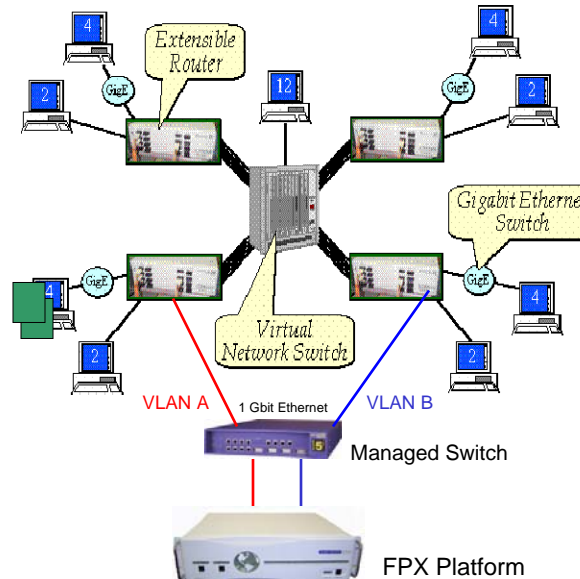
GUI to Install New Hardware Module

- Allows uploading and downloading of full or partial bitfiles
- Allows user to select a bitfile for programming
- FPGA reconfigures when user presses 'Execute Command'



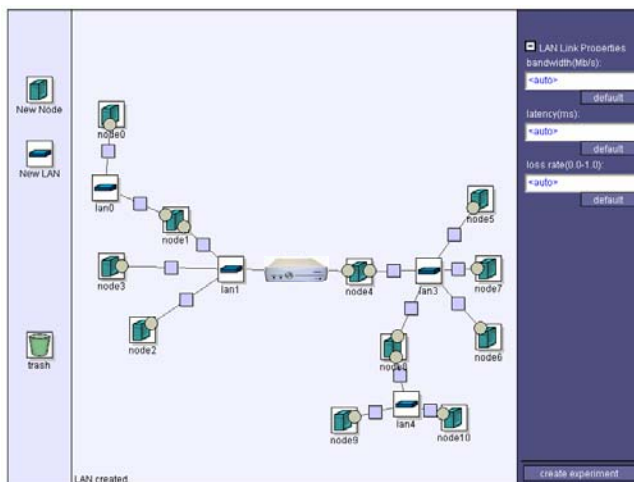
FPX Integration with ONL Testbed at WashU

- **Default ONL**
 - Reserve 1 or more Extensible Routers
- **Establish alternate path between Extensible Routers**
 - Create VLANs from 2 Extensible Routers to managed switch
- **FPX Integration**
 - Route traffic from VLAN A to VLAN B passing through FPX



FPX Integration with DETER

- **Insert FPX technology between nodes or networks**
- **FPX behaves as a generic reconfigurable node with 3 interfaces**
 - 1 Control Interface
 - 2 Gigabit Ethernet Ports



Acknowledgements

• Washington University :

- Faculty
 - John Lockwood (PI) (Reconfigurable Network Group)
 - Jon Turner (Applied Research Lab)
 - Ron Cytron (Distributed Object Computing)
- Graduate Students
 - Todd Sproull
 - Sarang Dharmapurikar
 - Haoyu Song
 - David Lim
 - James Moscola
 - David Schuehler (Now at)
 - Chris Zuver (Now at Boeing)
 - Bharath Madhusudan
 - Mike Attig (Now at Xilinx Labs)
 - Chris Neely (Now at Xilinx Labs)
 - Henry Fu (Continued @ Stanford)
- Undergraduate Students
 - Harvey Ku (at CMU)
 - Eliot Sinclair
 - Doug Stirrut
 - Tucker Evans (Now at General Dynamics)
 - Mike Wrighton (Now at CalTech)



• University Research Partners

- Ken Calvert (University of Kentucky)
- Matt Sanders (Georgia Tech)
- Ron Srodawa (Oakland University)
- Kuo-Tung Kuo (University of Maryland)
- Cary Colwell (Naval Postgraduate School)
- John Gibson (Naval Postgraduate School)
- Sven Shepstone (Cape Town)

• Visiting Faculty and Students

- Edson Horta (Univ. de Sao Paulo, Brasil)
- Florian Braun (University of Stuttgart)
- Carlos Macian (University of Stuttgart)
- Young Cho (UCLA / Berkeley)

• Industry Research Partners

- National Science Foundation
- SAIC
- Agilent Technologies
- Boeing
- Global Velocity
- Synplicity
- Xilinx



- **More Information :** <http://www.arl.wustl.edu/projects/fpx/reconfig.htm>