MOSFET Analytical Substrate Current Model for Circuit Simulation

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ABSTRACT

The MOSFET (metal-oxide-silicon field-effect transistor) substrate current has been expected to increase dramatically due to the transistor size shrinkage in a deep-submicron process (transistor channel length below or equal to 0.25 μm). This is a major concern for the accuracy of the existing models in predicting the transistor channel current and degradation of the device life-time, [1]. The main source for this substrate current increase is the hot-carrier effect, impact ionization. Most of the existing impact ionization rate models are accurate; however they require numerical analysis to determine the final solutions, [2-4]. The numerical methods applications in semiconductor device modeling are mostly limited at the device simulation level. For circuit analysis application, analytical solutions are preferred because of their simplicity and computational speed. In [5, 6], the Gauss-Laguerre integration method is shown to be effective in determining an accurate compact analytical model for the impact ionization rate. In this paper we apply same method, Gauss-Laguerre, on the substrate current model equation of [7], and the accuracy of our final analytical model is determined by comparing it with a well known compact analytical substrate model equation, [1] in the fitting of data from a 90nm device [11].

Keywords: impact ionization, substrate current, hot-electrons.

I. INTRODUCTION

Impact ionization (II) is one of the most important phenomena limiting the performance of submicron MOSFET devices. The substrate current resulting from impact ionization events, especially near the drain region, is correlated with device performance and can be used to monitor degradation. The substrate current in an n-channel MOSFET is given by

$$I_{sub} = I_{ds} \int_0^{l_d} \alpha_n dy \tag{1}$$

I_{ds} is the drain current, l_d is the length of the pinch-off region and α_n is the electron impact ionization coefficient in the velocity saturated part of the channel. This coefficient is a function of the channel electric field E and is usually modeled by the simple phenomenological expression

$$\alpha_n(E) = A_n e^{-\frac{B_n}{E}} \tag{2}$$

The parameters A_n, B_n are called the ionization constants. For silicon at room temperature $A_n \approx 7.03\times10^5$ cm^{-1} and $B_n = 1.23\times10^6$ V cm^{-1}. Substituting (2) into (1) yields the expression

$$I_{sub} = I_{ds0} A_n \int_0^{l_d} e^{-\frac{B_n}{E}} dy \tag{3}$$

If y is the distance along the channel measured from the start of the velocity saturated region where $E = E_{sat}$ quasi two-dimensional models suggest the formula

$$E(y) = E_{sat} \cosh(\frac{y}{l_d}) \qquad l_d = \sqrt{\frac{\varepsilon_{Si}}{\varepsilon_{ox}} x_j t_{ox}} \tag{4}$$

The parameter x_j is the drain junction depth and t_{ox} is the oxide thickness. If (4) is substituted into (3) and the integration variable is changed from y to $E(y)$ equation (3) becomes

$$I_{sub} = I_{ds} A_n l_d \int_{E_{sat}}^{E_{max}} \frac{1}{\sqrt{E^2 - E_{sat}^2}} e^{-\frac{B_n}{E}} dE \tag{5}$$

The integral can be approximated [8] by

$$I_{sub} = \frac{I_{ds} A_n l_d E_{max}^2 e^{-\frac{B_n}{E_{max}}}}{B_n \sqrt{E_{max}^2 - E_{sat}^2}} \approx I_{ds} \frac{A_n l_d E_{max}}{B_n} e^{-\frac{B_n}{E_{max}}} \tag{6}$$

The maximum value E_{max} of E occurs at the drain and can be approximated by

$$E_{max} = \frac{V_{ds} - V_{dsat}}{l_d} \tag{7}$$

Both l_d and the saturation voltage V_{dsat} are dependent on the gate voltage V_g . For a MOSFET of length L, a simple formula for V_{dsat} is given by

$$V_{dsat} = \frac{V_g - V_{th}}{\alpha + \mu(V_g - V_{th})/2Lv_{sat}} \qquad (8)$$

The saturation velocity in silicon is approximately $v_{sat} = 10^7$ cm s^{-1} and $E_{sat} \approx 6.7 \times 10^4 V$ cm^{-1}. Typical parameters values are $\alpha = 1.2$ and $\mu = 300$ cm^2 V^{-1}s^{-1}. Combining (4)-(8) gives the simple formula

$$I_{sub} = I_{ds} \frac{A_n}{B_n}(V_{ds} - V_{dsat}) e^{-\frac{l_d B_n}{V_{ds} - V_{dsat}}} \qquad (9)$$

For a nanometer scale device $l_d B_n \approx 3\ V$ and $A_n / B_n \approx 0.57$. The form of $\alpha_n(E)$ given by (2), and the drain field approximation (7) are the key ingredients in the substrate current formulae used in SPICE models. In the following sections we will examine these two aspects and propose some device physics based alternatives.

II. THE IMPACT IONIZATION RATE

Impact ionization (II) in submicron silicon devices subjected to high electric field is related to the behavior of the hot-electron sub-population with energies above the II threshold energy $\varepsilon_{th} \approx \varepsilon_g = 1.2$ ev. In a MOSFET device II events occur in a region about the drain and the substrate current flows to the base as illustrated schematically in Figure 1.

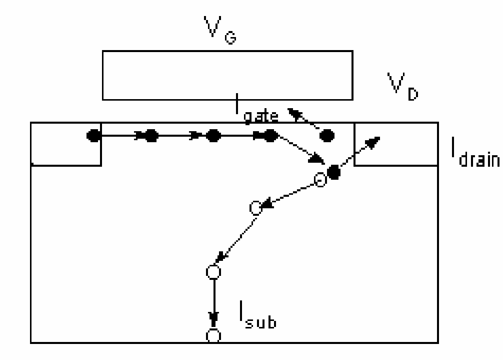

Figure 1.The MOSFET substrate current

We assume that the hot-electron distribution function has the Maxwellian form

$$f(\varepsilon) = n\left(\frac{\hbar^2}{2\pi m^* \theta}\right)^{\frac{3}{2}} e^{-\frac{\varepsilon}{\theta}} \qquad (10)$$

The parameter θ is the hot-electron temperature and is taken to be dependent upon the electric field strength E .

Equation (10) leads to the Scholl-Quade formula impact ionization formula [9].

$$G_{ii}(n,u) = \frac{n}{\tau_0 \sqrt{\pi}} F_{exact}(u)$$

$$F_{exact}(u) = \sqrt{u}\exp\left(-\frac{1}{u}\right) - \sqrt{\pi}\,\mathrm{erfc}\left(\frac{1}{\sqrt{u}}\right) \qquad (11)$$

$$u = \frac{\theta}{\varepsilon_{th}}$$

This is a closed form, but inconvenient, representation for practical device modeling. In [6] we showed that by using Gauss-Laguerre integration [5-6] $G_{ii}(n,u)$ can be expressed in the form

$$G_{ii}(n,u) = \frac{n}{\tau_0 \sqrt{\pi}} e^{-\frac{1}{u}} F(u)$$

$$F(u) = \sqrt{u} - \sum_{k=1}^{\infty} w_k \frac{1}{\sqrt{x_k + u^{-1}}} \qquad (12)$$

The constant $\tau_0 \approx 1.26 \times 10^{-14}$ and $\{w_k\}_{k=1}^{\infty}, \{x_k\}_{k=1}^{\infty}$ are the weight and nodal coefficients of the Gauss-Laguerre algorithm. Figure 2 shows a comparison between the exact result (11) with the approximation (12) using a 5-term expansion. For most applications a 3-term approx is adequate due to the small exponential factor

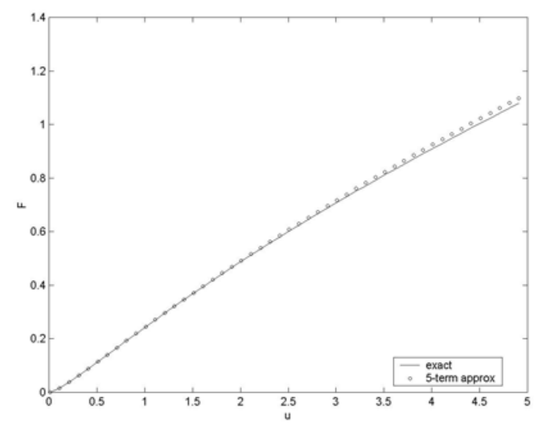

Figure 2. The 5 term-approx to $F(u)$ compared to $F_{exact}(u)$

The function F_{exact} has the asymptotic behavior

$$F_{exact}(u) \sim \begin{cases} 0.5\sqrt{u^3} & u \sim 0 \\ \sqrt{u} & u \sim \infty \end{cases} \qquad (13)$$

However neither term alone provides an adequate approximation. The importance of (12) lies in the fact that we have been able to factor out the exponential term at the same time as providing analytic approximations. This makes it suitable for the construction of compact substrate current models. In the drain region, where we assume the impact ionization events are occurring, the ionization rate G_{ii} and the impact ionization coefficient α_n are related by $G_{ii} = nv_{sat}\alpha_n$ and this gives us the formula

$$\alpha_n = \frac{1}{\tau_0 v_{sat}\sqrt{\pi}} e^{-\frac{\varepsilon_{th}}{\theta(E)}} F(\frac{\theta(E)}{\varepsilon_{th}}) \qquad (14)$$

To complete the model we must model the temperature function $\theta(E)$. If we assume the linear relation

$$\theta(E) = \frac{\varepsilon_{th}}{B_n} E \qquad (15)$$

(14) gives

$$\alpha_n = A_n(E) e^{-\frac{B_n}{E}}$$
$$A_n(E) = \frac{1}{\tau_0 v_{sat}\sqrt{\pi}} F(\frac{E}{B_n}) \qquad (16)$$

This generalizes (2) and the analog of (7) is

$$I_{sub} = I_{ds} A_n(E_{\max}) l_d E_{\max} e^{-\frac{B_n}{E_{\max}}}$$
$$E_{\max} = \frac{V_{ds} - V_{dsat}}{l_d} \qquad (17)$$

The relationship (15) is an approximation that yields the currently accepted impact coefficient formula (2). Several other formulae have been proposed. In this paper we assume the linear model

$$\theta(E) = \theta_0 + \frac{\varepsilon_{th}}{B_n} E \qquad (18)$$

to replace (15). This is a simplification of the form

$$\theta(E) = \theta_0 + \theta_1 E + \theta_2 E^2 \qquad (19)$$

proposed by Thornber [10]. The parameters in (19) are dependent on the lattice temperature T which is important in understanding the temperature dependence of the substrate current. Our model is defined by two parameters and has the generic form

$$V_{dsat} = \frac{V_g - V_{th}}{p_2 + p_3(V_g - V_{th})}$$
$$u = p_4 + \frac{V_{ds} - V_{dsat}}{p_5} \qquad (20)$$
$$I_{sub} = I_{ds} p_1 (V_{ds} - V_{dsat}) F(u) e^{-\frac{1}{u}}$$

The model has three parameters, p_1, p_4, p_5 that are specific substrate current parameters.

III. RESULTS

Figure 3 shows a schematic of a 90nm MOSFET device. Data for this device is available on the internet [11]. The I-V characteristics as well as substrate current values are provided.

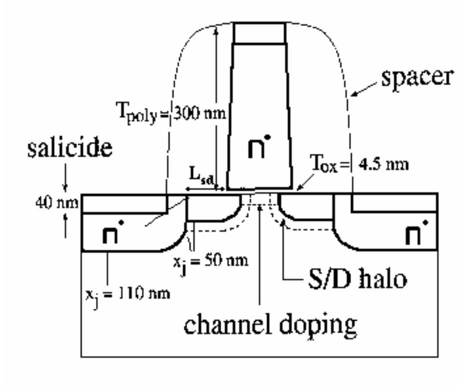

Figure3. A 90nm MOSFET device

For this device (4) gives the estimate $l_d = 2.61 \times 10^{-6}$ cm. The device has a width of 49.4 microns but all the data is width normalized. Figure 4 shows the current voltage curves for the device.

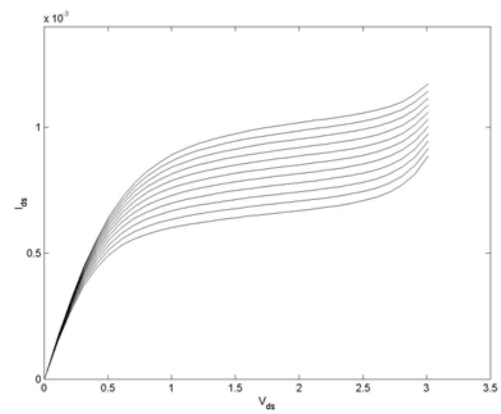

Figure 4. The I-V characteristics for gate voltages 0.01-3.01V

The dependence of I_{ds} as a function of V_g for low values of V_{ds} is used to obtain the estimates of V_{th} and μ. Using these values in (8) we get

$$V_{dsat} = \frac{V_g - V_{th}}{1.2 + 0.85(V_g - V_{th})} \qquad (21)$$

The formula for the substrate current is relatively insensitive to the saturation voltage and (21) is adequate. The values of

p_2, p_3 in (20) are allowed to float as part of a parameter optimization scheme and so the values in (21) simply provide initial values. From (17) we observe that I_{sub}/I_{ds} allows direct access to $F(u)$. Equation (9) can be written in the form

$$\gamma \doteq \ln\left(\frac{I_{sub}}{I_{ds}}\frac{1}{(V_{ds}-V_{dsat})}\right) = \ln\left(\frac{A_n}{B_n}\right) - \frac{l_d B_n}{V_{ds}-V_{dsat}} \quad (22)$$

If the usual model is correct, a plot of γ against $(V_{ds}-V_{dsat})^{-1}$ should be a straight line from which the quantity $l_d B_n$ can be estimated.

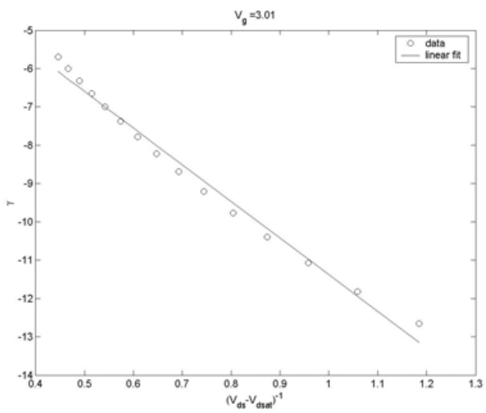

Figure 5. The circles are the data points and the solid line is a linear fit to the data for a gate voltage of 3.01 V.

The curves show a definite curvature indicating that the usual model is not adequate. This could be due to strong dependence of l_d on the excess voltage $(V_{ds}-V_{dsat})$ but we ascribe it to a failure of the original model (9). From these plots we obtain the parameter estimate $B_n l_d = 12.8V$.

Using this value together with a standard optimization method the fits in Figure 6 were obtained.

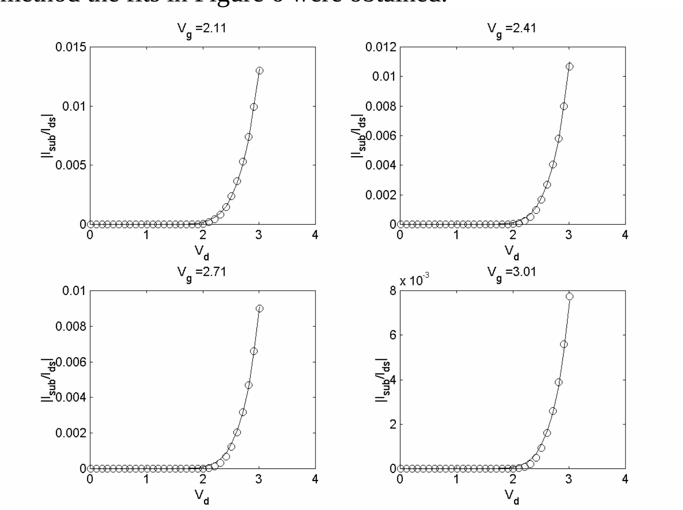

Figure 6. Some examples of fits using our new model

IV. Conclusion

We have demonstrated that the usual MOSFET substrate current model fails for a 90nm device and have presented a new model and shown that it can be fitted to the data. As device lengths shorten still further we believe our simple modifications will be of increasing importance.

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