

## **Jeffrey T. Draper**

Research Assistant Professor, Ming Hsieh Department of Electrical Engineering  
Project Leader, Information Sciences Institute  
University of Southern California  
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### **RESEARCH INTERESTS**

Radiation-Hardening by Design, Processing-in-Memory, Networks-on-Chip, Computer Architecture, VLSI

### **EDUCATION**

UNIVERSITY OF TEXAS, AUSTIN, TX

Ph.D. in Computer Engineering, May 1993, GPA: 4.0/4.0

Thesis: *Efficient Message Transport in Multicomputer Systems*

Supervising Professor: Dr. Joydeep Ghosh

M.S.E. in Computer Engineering, August 1990, GPA: 4.0/4.0

Thesis: *The M-Cache: A Message Cache for Message-Passing Multicomputers*

Supervising Professors: Dr. William Athas and Dr. Joydeep Ghosh

TEXAS A&M UNIVERSITY, COLLEGE STATION, TX

B.S. in Electrical Engineering, May 1987, GPA: 4.0/4.0

Specialization: Microprocessor Systems

### **WORK EXPERIENCE**

July 1993 to Present

UNIVERSITY OF SOUTHERN CALIFORNIA

INFORMATION SCIENCES INSTITUTE, MARINA DEL REY, CALIFORNIA

MING HSIEH DEPARTMENT OF ELECTRICAL ENGINEERING, LOS ANGELES, CALIFORNIA

Titles: Research Assistant Professor, Project Leader, Computer Scientist

Directed VLSI efforts of several DARPA-funded projects. Developed ASIC test articles for the Trusted Integrated Circuits program. Contributed to the architecture design of polymorphous computing architectures and co-led the VLSI implementation of a representative chip in IBM 90nm technology that contained on the order of 100 million gates. Directed the VLSI development of two prototype 64Kbit SRAM chips to demonstrate radiation-hardening-by-design principles. Contributed to the architecture design of processor-in-memory chips (PIM) based on embedded DRAM technology and led the corresponding VLSI implementation efforts that produced two 55-million transistor PIM chips: one integer-based and one enhanced with single-precision floating-point units. Developed a routing algorithm for ring structures which yields lower latency and more throughput than previous research. Supervised the work of several PhD and MS graduate students and served on numerous PhD qualifier and defense committees. Helped administer PhD screening exams. Taught EE577B - VLSI Design Project several semesters.

January 1991 to May 1993

UNIVERSITY OF TEXAS, AUSTIN, TEXAS

Title: Research Assistant

Developed an analytical model for predicting performance measures of message transport in multicomputers. Devised new schemes for message handling and routing in multicomputers and

implemented simulation tools to evaluate the schemes. Performed system administration tasks on IBM RS/6000 workstations.

September 1990 to May 1991  
UNIVERSITY OF TEXAS, AUSTIN, TEXAS

Title: Teaching Assistant

Served as a proctor, test administrator, and grader in the class entitled "Fundamentals of Logic Design". Lectured for introductory sessions and tutored students.

June 1987 to August 1988 and Summer 1986  
GENERAL DYNAMICS, FT. WORTH, TEXAS

Titles: Engineer, Engineering Intern

Designed and built MC68000-based single-board computers to serve as control units for various projects. Utilized a CAD system to draw circuits for avionics tester equipment. Edited software for simulation runs on these testers.

## HONORS

Fellowships:

Engineering Foundation 1990 – 1991, Microelectronics & Computer Development 1988 – 1990

Scholarships 1983 – 1987:

McFadden, McDermott, Fasken Foundation, UIL Joe B. Cooke

Honor Societies:

Phi Kappa Phi, Tau Beta Pi, Eta Kappa Nu, Phi Eta Sigma

Awards:

Outstanding Junior in the College of Engineering 1986,  
Gathright Academic Excellence Award 1986, Dean's List 1983 – 1987

## AFFILIATIONS

IEEE, IEEE Computer Society, Tau Beta Pi, Eta Kappa Nu

## PROFESSIONAL SERVICES

Conducted 2-day short course on Processing-in-Memory (PIM) technology at National Chiao Tung University. Reviewed articles for *IEEE Transactions on Computers*, *IEEE Transactions on Parallel and Distributed Systems*, *Journal of Parallel and Distributed Computing*, and numerous conferences. Reviewed a tutorial for IEEE Computer Society Press. Chaired sessions at several conferences. Served on National Science Foundation proposal review panel.

## JOURNAL PUBLICATIONS

- Michael Bajura, et al, "Models and Algorithmic Limits for an ECC-Based Approach to Hardening Sub-100nm SRAMs," *IEEE Transactions on Nuclear Science*, Vol 54, Number 4, August 2007, pp. 935 - 945
- Sumit Mediratta, Jeffrey Draper, "Achieving On-chip Fault-tolerance Utilizing BIST Resources," *WSEAS Transactions on Circuits and Systems*, Vol 5, No 12, December 2006, pp. 1726 – 33
- Jeffrey Draper, et al, "A Prototype Processing-In-Memory (PIM) Chip for the Data-Intensive Architecture (DIVA) System," *Journal of VLSI Signal Processing*, Vol 40, No 1, May 2005, pp. 73 – 84

- Joong-Seok Moon, et al, "Voltage-Pulse Driven Harmonic Resonant Rail Drivers for Low-Power Applications," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, Vol 11/5, October 2003, pp. 762 – 77
- Herming Chiueh, Jeffrey Draper, John Choma, Jr., "A Dynamic Thermal Management Circuit for System-On-Chip Designs," *Analog Integrated Circuits and Signal Processing*, Vol 36/1-2, July - August 2003, pp. 175 – 81
- Herming Chiueh, Jeffrey Draper, John Choma, Jr., "A Programmable Thermal Management Interface Circuit for PowerPC Systems," *Microelectronics Journal*, Vol 32/10-11, pp. 875 - 81
- Louis Luh, John Choma, Jr., and Jeffrey Draper, "A High-Speed Fully Differential Current Switch," *IEEE Transactions on Circuits and Systems*, April 2000, pp. 358 – 63
- Louis Luh, John Choma, Jr., and Jeffrey Draper, "A Continuous-Time Common-Mode Feedback Circuit (CMFB) for High-Impedance Current-Mode Applications," *IEEE Transactions on Circuits and Systems*, April 2000, pp. 363 – 9
- Jeffrey T. Draper and Joydeep Ghosh, "A Comprehensive Analytical Model for Wormhole Routing in Multicomputer Systems," *Journal of Parallel and Distributed Computing*, November 1994, pp. 202 – 14
- Jeffrey T. Draper and Joydeep Ghosh, "The M-Cache: A Message-Handling Mechanism for Multicomputer Systems," *Parallel Computing*, September 1994, pp. 1269 – 88
- Joydeep Ghosh, Kelvin Goveas, and Jeffrey T. Draper, "Performance Evaluation of a Parallel I/O Subsystem for a Hypercube Multicomputer," *Journal of Parallel and Distributed Computing*, January 1993, pp. 190 – 206

## CONFERENCE PAPERS/PRESENTATIONS

- Taek-Jun Kwon, Jeff Sondeen, Jeffrey Draper, Floating-Point Division and Square Root using a Taylor-Series Expansion Algorithm, *Proceedings of the 50th IEEE International Midwest Symposium on Circuits and Systems*, August 2007, pp. 305 - 308
- Young Hoon Kang, Jeffrey Draper, Design Trade-offs for Load/Store Buffers in Embedded Processing Environments, *Proceedings of the 50th IEEE International Midwest Symposium on Circuits and Systems*, August 2007, pp. 1461 - 1464
- Rashed Zafar Bhatti, Monty Denneau, Jeff Draper, Data Strobe Timing of DDR2 using a Statistical Random Sampling Technique, *Proceedings of the 50th IEEE International Midwest Symposium on Circuits and Systems*, August 2007, pp. 1114 - 1117
- Rashed Zafar Bhatti, Keith Chugg, Jeff Draper, Standard Cell based Pseudo-Random Clock Generator for Statistical Random Sampling of Digital Signals, *Proceedings of the 50th IEEE International Midwest Symposium on Circuits and Systems*, August 2007, pp. 1110 - 1113
- Sumit Mediratta, Jeffrey Draper, Performance Evaluation of Probe-Send Fault-tolerant Network-on-Chip Router, *Proceedings of the IEEE International Conference on Application-Specific Systems, Architectures, and Processors*, July 2007, pp. 69 - 75
- Riaz Naseer, et al, Critical Charge Characterization for Soft Error Rate Modeling in 90nm SRAM, *Proceedings of the IEEE International Symposium on Circuits and Systems*, May 2007, pp. 1879 - 1882
- Sumit Mediratta, Jeffrey Draper, Characterization of a Fault-tolerant NoC Router, *Proceedings of the IEEE International Symposium on Circuits and Systems*, May 2007, pp. 381 - 384

- Riaz Naseer, et al, Critical Charge and SET Pulse Widths for Combinational Logic in Commercial 90nm CMOS Technology, *Proceedings of the 2007 ACM Great Lakes Symposium on VLSI*, March 2007, pp. 227 - 230
- Sumit Mediratta, Jeffrey Draper, Effective Realization of On-chip Fault-tolerance Utilizing BIST Resources, *Proceedings of the 5th WSEAS Int. Conf. on Circuits, Systems, Electronics, Control & Signal Processing*, November 2006
- Riaz Naseer, Rashed Zafar Bhatti, Jeff Draper, Analysis of Soft Error Mitigation Techniques for Register Files in IBM Cu-08 90nm Technology, *Proceedings of the 49th IEEE International Midwest Symposium on Circuits and Systems*, August 2006
- Sumit Mediratta, Jeffrey Draper, On-chip Fault-tolerance Utilizing BIST Resources, *Proceedings of the 49th IEEE International Midwest Symposium on Circuits and Systems*, August 2006
- Rashed Zafar Bhatti, Craig Steele, Jeff Draper, PBuf: An On-Chip Packet Transfer Engine for MONARCH, *Proceedings of the 49th IEEE International Midwest Symposium on Circuits and Systems*, August 2006
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- Rashed Bhatti, Monty Denneau, Jeff Draper, Phase Measurement and Adjustment of Digital Signals Using Random Sampling Technique, *Proceedings of the IEEE International Symposium on Circuits and Systems*, May 2006, pp. 3886 – 9
- Tim Barrett, et al, A Double-Data Rate (DDR) Processing-in-Memory (PIM) Device with WideWord Floating-Point Capability, *Proceedings of the IEEE International Symposium on Circuits and Systems*, May 2006, pp. 1933 – 6
- Rashed Zafar Bhatti, Monty Denneau, Jeff Draper, 2 Gbps SerDes Design Based on IBM Cu-11 (130nm) Standard Cell Technology, *Proceedings of the 2006 ACM Great Lakes Symposium on VLSI*, May 2006, pp. 198 – 203
- Sumit Mediratta, Jeffrey Draper, Performance Analysis of User-Level PIM Communication in the Data-Intensive Architecture (DIVA) System, *Proceedings of the 12th International Conference on High Performance Computing (HiPC 2005)*, December 2005, pp. 407 – 19
- Rashed Zafar Bhatti, Monty Denneau, Jeff Draper, Duty Cycle Measurement and Correction Using a Random Sampling Technique, *Proceedings of the 48th IEEE International Midwest Symposium on Circuits and Systems*, August 2005
- Riaz Naseer, Jeff Draper, The DF-DICE Storage Element for Immunity to Soft Errors, *Proceedings of the 48th IEEE International Midwest Symposium on Circuits and Systems*, August 2005
- Taek-Jun Kwon, Jeff Sondeen, Jeff Draper, Design Trade-Offs in Floating-Point Unit Implementation for Embedded and Processing-In-Memory Systems, *Proceedings of the IEEE International Symposium on Circuits and Systems*, May 2005, pp. 3331 – 4
- Sumit Mediratta, Craig Steele, Jeff Sondeen, Jeffrey Draper, An Area-Efficient and Protected Network Interface for Processing-In-Memory Systems, *Proceedings of the IEEE International Symposium on Circuits and Systems*, May 2005, pp. 2951 – 4
- Sumit Mediratta, Craig Steele, Ravinder Singh, Jeff Sondeen, Jeffrey Draper, A 0.18um CMOS Implementation of an Area Efficient Precise Exception Handling Unit for Processing-In-Memory Systems, *Proceedings of the 47th IEEE International Midwest Symposium on Circuits and Systems*, July 2004, Vol. III, pp. 455 – 58
- Taek-Jun Kwon, Joong-Seok Moon, Jeff Sondeen, Jeff Draper, A 0.18um Implementation of a Floating-Point Unit for a Processing-In-Memory System, *Proceedings of the IEEE International Symposium on Circuits and Systems*, May 2004, Vol. II, pp. 453 – 56

- Sumit Mediratta, Jeff Sondeen, Jeffrey Draper, An Area-Efficient Router for the Data-Intensive Architecture (DIVA) System, *Proceedings of the 17th International Conference on VLSI Design* , January 2004
- Joong-Seok Moon, Taek-Jun Kwon, Jeff Sondeen, Jeff Draper, An Area-Efficient Standard-Cell Floating-Point Unit Design for a Processing-In-Memory System, *Proceedings of the 29th European Solid-State Circuit Conference* , September 2003
- Jeffrey Draper, Jeff Sondeen, Chang Woo Kang, Implementation of a 256-bit WideWord Processor for the Data-Intensive Architecture (DIVA) Processing-In-Memory (PIM) Chip, *Proceedings of the 28th European Solid-State Circuit Conference* , September 2002
- Herming Chiueh, Jeffrey Draper, Sumit Mediratta, Jeff Sondeen, The Address Translation Unit of the Data-Intensive Architecture (DIVA) System, *Proceedings of the 28th European Solid-State Circuit Conference* , September 2002
- Jeffrey Draper, Jeff Sondeen, Sumit Mediratta, Ihn Kim, Implementation of a 32-bit RISC Processor for the Data-Intensive Architecture Processing-In-Memory Chip, *Proceedings of the IEEE International Conference on Application-Specific Systems, Architectures, and Processors*, July 2002
- Jeff Draper, et al, The Architecture of the DIVA Processing-In-Memory Chip, *Proceedings of the International Conference on Supercomputing*, June 2002
- Joong-Seok Moon, William C. Athas, Peter A. Beerel, Jeffrey T. Draper, Low-Power Sequential Access Memory Design, *Proceedings of the IEEE Custom Integrated Circuits Conference*, May 2002
- Herming Chiueh, Jeffrey Draper, John Choma, Jr., A Dynamic Thermal Management Circuit for System-on-Chip Designs, *Proceedings of the International IEEE Conference on Electronics, Circuits, and Systems*, September 2001
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- Herming Chiueh, Jeffrey Draper, John Choma, Jr., A Programmable Thermal Management Interface Circuit for PowerPC Systems, *Proceedings of the 6th International Workshop on Thermal Investigation of ICs and Systems*, September 2000
- Louis Luh, John Choma, Jr., Jeffrey Draper, A 400MHz 5th-Order CMOS Continuous-Time Switched-Current Sigma-Delta Modulator, *Proceedings of the European Solid-State Circuits Conference*, September 2000
- Herming Chiueh, Jeffrey Draper, and John Choma, Jr., Implementation of a Temperature Monitoring Interface Circuit for PowerPC Systems *Proceedings of the IEEE Midwest Symposium on Circuits and Systems*, August 2000
- Chang Woo Kang and Jeffrey Draper, A Fast, Simple Router for the Data-Intensive Architecture (DIVA) System, *Proceedings of the IEEE Midwest Symposium on Circuits and Systems*, August 2000
- Louis Luh, Jeffrey Draper, and John Choma, Jr., Performance Optimization for High-Order Continuous-Time Sigma-Delta Modulators with Extra Loop Delay, *Proceedings of the IEEE International Symposium on Circuits and Systems*, May 2000
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- Herming Chiueh, Jeffrey Draper, and John Choma, Jr., A Novel Fully Integrated Fan Controller for Advanced Computer Systems *Proceedings of the Southwest Symposium on Mixed-Signal Design*, February 2000
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- Louis Luh, John Choma, and Jeffrey Draper, Area-Efficient Area Pad Design for High Pin-Count Chips, *Proceedings of the Great Lakes Symposium on VLSI*, March 1999, pp. 78 – 81
- Herming Chiueh, Jeffrey Draper, Louis Luh, and John Choma, A Novel Model for On-Chip Heat Dissipation, *Proceedings of the 1998 IEEE Asia-Pacific Conference on Circuits and Systems*, November 1998, pp. 779 – 82
- Louis Luh, John Choma, and Jeffrey Draper, A Continuous-Time Common-Mode Feedback Circuit (CMFB) for High-Impedance Current-Mode Application, *Proceedings of the 5th IEEE International Conference on Electronics, Circuits, and Systems*, September 1998, Vol. 3, pp. 347 – 50
- Louis Luh, John Choma, and Jeffrey Draper, A High-Speed Fully Differential Current Switch, *Proceedings of the 5th IEEE International Conference on Electronics, Circuits, and Systems*, September 1998, Vol. 3, pp. 343 – 6
- Herming Chiueh, Jeffrey Draper, Louis Luh, and John Choma, A Thermal Evaluation of Integrated Circuits: On-Chip Offset Temperature Measurement and Modeling, *Proceedings of the Second International Workshop on Design of Mixed-Mode Integrated Circuits and Applications*, July 1998, pp. 109 – 13
- Louis Luh, John Choma, and Jeff Draper, A 50MHz Continuous-Time Switched-Current Sigma Delta Modulator, *Proceedings of the 1998 IEEE International Symposium on Circuits and Systems*, June 1998, Vol. I, pp. 579 – 82
- Craig S. Steele, Jeff Draper, and Jeff Koller, SafetyNet: Secure Communications for Embedded High-Performance Computing, *Lecture Notes in Computer Science 1388 (IPPS/SPDP'98 Workshops Proceedings)*, April 1998, pp. 908 – 12
- Jeff Draper, Jay Block, Jeff Koller, and Craig Steele, Thermal Management in Embedded Systems Using MEMS, *Lecture Notes in Computer Science 1388 (IPPS/SPDP'98 Workshops Proceedings)*, April 1998, pp. 900 – 1
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- Craig S. Steele, Jeff Draper, Jeff Koller, and Claire LaCour, A Bus-Efficient Low-Latency Network Interface for the PDSS Multicomputer, *Proceedings of the International Symposium on High Performance Distributed Computing*, August 1997, pp. 213 – 22
- Jeff Draper and Fabrizio Petrini, Routing in Bidirectional k-ary n-cubes with the Red Rover Algorithm, *Proceedings of the International Conference on Parallel and Distributed Processing Techniques and Applications*, June 1997, pp. 1184 – 93
- J. Koller, J. Block, J. Draper, C. Lacour, and C. Steele, Lessons from Three Generations of Embeddable Supercomputers, Presented at the Second International Workshop on Embedded HPC Systems and Applications, Geneva, Switzerland, April 1997

- Jeff Draper, The Red Rover Algorithm for Deadlock-Free Routing on Bidirectional Rings, *Proceedings of the International Conference on Parallel and Distributed Processing Techniques and Applications*, August 1996, pp. 345 – 54
- Jeffrey T. Draper and Joydeep Ghosh, Multipath E-Cube Algorithms (MECA) for Adaptive Wormhole Routing and Broadcasting in k-ary n-cubes, *Proceedings of the Sixth International Parallel Processing Symposium*, March 1992, pp. 407 – 10
- Jeffrey T. Draper, Joydeep Ghosh, and William C. Athas, The M-Cache: A Message-Retrieving Mechanism for Multicomputer Systems, *Proceedings of the IEEE Symposium on Parallel and Distributed Processing*, December 1991, pp. 258 – 65

## ACTIVE RESEARCH PROJECTS

Trusted Integrated Circuits (TIC), DARPA, October 2007 – present

The DARPA TIC program has observed the trend of foundries and design houses moving off-shore. The program is attempting to develop techniques for guaranteeing that the devices that come back from fabrication identically match the designs submitted, specifically that no “Trojan horses” have been inserted to the design. While obvious national security issues are involved in such a paradigm, in an academic sense, the program involves techniques for demonstrating proofs of correctness. Our primary role on the program is to provide ASIC test chips that can serve as testbeds for demonstrating such techniques. The program is a phased program starting with smaller ASICs and building up billion-transistor chips by the final phase. Multi-core and network-on-chip architecture research will be involved in the final phases. We have recently completed the fabrication of Test Article 0, a single-precision floating-point unit, in IBM 90nm technology.

Radiation-Hardening-by-Design (RHBD), DARPA, January 2006 – present

The main thrust of the RHBD program is to use architecture, circuit design, and layout techniques to build chips that are radiation-tolerant by using commodity commercial foundry lines. This approach is becoming highly desired because radiation-hard foundries are becoming prohibitively expensive and the technologies they support tend to lag behind state-of-the-art by two or three generations. In initial experiments we have designed 64Kbit SRAM chips using RHBD techniques and have fabricated two such chips: one in IBM 9LP 90nm technology and the other in IBM 9SF 90nm technology. Radiation tests have shown that these chips perform with respect to single-event effects and are also capable of performing with high total ionizing doses (greater than 300 Krads). Further testing has shown that high-temperature treatments produces an annealing effect that restores previously irradiated chips to their pre-irradiated state.

## COMPLETED RESEARCH PROJECTS

Morphable Networked Architectures (MONARCH), DARPA, June 2001 – March 2007

The MONARCH project is investigating polymorphous computing architectures that can adapt underlying computing structures to perform efficient computing in response to algorithm needs or even stimuli from the environment. The MONARCH architecture will support reactive multi-mission, multi-sensor, and in-flight retargetable missions. In support of this project, DIVA PIM technology is being integrated with a Raytheon streaming architecture design to implement a polymorphic computing platform. A MONARCH chip measuring over 18mm on a side has been fabricated in IBM 90nm technology and is currently in test.

Cognitive Engine Technologies (COGENT), DARPA, August 2004 - July 2006

COGENT is a multidisciplinary effort to study, develop, and evaluate concepts for an advanced cognitive information processing architecture. The COGENT architecture will exploit advances in problem solving approaches, computer architecture, power management, storage techniques and even relevant new technologies to achieve substantial improvements in cognitive processing throughput.

PIM Technology for Knowledge Discovery, AFRL, August 2004 - November 2005

This project explored the use of processing-in-memory (PIM) technology to speed up algorithms used in knowledge discovery applications. Besides the analysis of algorithms, applications were ported to PIM systems developed under the DIVA and Godiva projects for benchmarking purposes. Based on these performance results, projections incorporating technology roadmaps were formulated to predict capabilities of mature PIM technology.

Cyclops SERDES Design, IBM T. J. Watson, September 2004 - January 2005

The IBM Cyclops project is building a multithreaded architecture for cellular computing. The VLSI devices incorporated in this architecture contain high-speed serial links for interconnecting devices. These links require serializers and deserializers (SERDES) to convert between the on-chip high-speed parallel buses and off-chip high-speed serial links. We developed a fully digital design to accomplish this requirement in less area and with lower power dissipation than alternatives.

Godiva, DARPA, August 2002 - February 2004

The Godiva project was a collaboration between USC, Hewlett-Packard Laboratories, and Rice University to investigate how processing-in-memory (PIM) technology could be applied to commercial systems. This project leveraged research from the Data-Intensive Architecture (DIVA) project. In addition to the basic research component of this project, a prototype system was developed that inserts processing-in-memory (PIM) devices with floating-point capability into the memory system of an HP Long's Peak server, which is based on the Itanium2 processor.

Data-Intensive Architecture (DIVA), DARPA, April 1998 - December 2002

The DIVA project explored the use of embedded DRAM technology to build smart memory coprocessors to a host microprocessor. By also using a separate memory-to-memory interconnect, DIVA exploits inherent bandwidth both on chip and across the system. DIVA supports familiar programming paradigms from parallel computing to target a broad range of applications. The DIVA project built a prototype system using VLSI PIM chips in place of standard DRAMs to demonstrate these concepts. The first prototype PIM chip contained 55-million transistors in a 10mm x 10mm silicon area and was fabricated in TSMC 0.18 $\mu$ m technology.

Integrated Thermal Management (ITEM), DARPA, October 1995 - June 1999

Innovative techniques for sensing and controlling thermal effects in high density scalable systems were developed, including the investigation of microelectromechanical devices. This capability provides great cost savings in design of a thermal management system for a computer, as it allows a system design that targets nominal power dissipation, rather than worst-case. The resulting system then actively monitors and controls itself to remain within that specification.

Advanced Scalable Network Technology (ASNT), DARPA, October 1995 - September 1999

The ASNT project exploited large numbers of chip pins offered by area pad technology to provide several networks in the same system, each customized for a specific function and/or message type. The idea was formulated from the observation that the message traffic on previous generations of multicomputers tended to be bimodal: messages were either short control-type messages or large messages for the transfer of huge blocks of data.

Packaging-Driven Scalable System (PDSS), DARPA, October 1994 - June 1997

PDSS is an embeddable multicomputer which utilizes area interconnect to achieve a high-bandwidth 1-dimensional network. This system architecture considerably simplifies interconnect while yielding better performance for systems up to 64 nodes. As part of this project, a custom VLSI chip containing 250,000 transistors and using area pad arrays to provide 555 signals was designed and fabricated. The Red Rover routing algorithm was also developed as part of this project.

Embeddable Variant (EV), DARPA, October 1992 - June 1995

The Embeddable Variant is an adaptation of the Intel Touchstone architecture using multichip module (MCM) technology. The finished system contained 16 nodes in a standard 27 cubic inch SEM-E package. This project involved a wide range of expertise, ranging from ASIC design to operating systems and parallel applications.

Modeling of Wormhole-Routed Networks

An analytical model based on queuing theory principles was developed for yielding latency and throughput measures of wormhole-routed networks. Application of the model to various networks revealed bottlenecks and quantified the effect of cascaded blocking.

MECA (Multi-path E-cube Algorithm)

An adaptive routing algorithm based on the dimension-ordered E-cube algorithm was devised. To evaluate the algorithm, a C++ program implementing a detailed network simulator was developed. This simulator was made available to the research community and subsequently used on the ATOMIC project at USC/ISI, which led to the founding of Myricom.

The M-Cache

The M-Cache is a hardware aid for message-driven programming paradigms. This work included hardware design, specification, performance evaluation, and implementation analysis of a technique for speeding up message handling in message-passing multicomputers.

## **REFERENCES**

Available upon request