TID Damage and Annealing Response of 90 nm Commercial-Density SRAMs

Y. Boulghassoul, M. Bajura, S. Stansberry, J. Draper, R. Naseer and J. Sondeen

***Abstract*— We characterize the TID resilience and annealing response of high-density SRAMs, fabricated in 90 nm commercial processes. Results demonstrate intrinsic SRAM hardness at 300 krad(Si), but also reveal several orders of magnitude increase in leakage current at 1 Mrad(Si) of exposure, with recorded critical functionality failures. However, the technology is shown to be very responsive to temperature treatments as all chips recover to pre-rad leakage levels after 5 hours at 150^{o}C with fully regained functionality. Finally, consecutive exposure/anneal cycles reveal a drastic improvement in TID resilience as SRAMs that did undergo at least one post-rad anneal stayed fully functional up to the strategic TID level of 2 Mrad(Si) once re-exposed. The gained resilience is attributed to negative interface trapped charge build-up along the STI walls: it progressively turns OFF the channel of parasitic transistors responsible for TID-induced leakage paths creation.**

***Index Terms*— Leakage current, SRAM, temperature annealing, total ionizing dose, 90 nm commercial process, interface traps.**

I. INTRODUCTION

THE resilience of commercial bulk CMOS processes to total ionizing dose (TID) damage has greatly benefited from the aggressive vertical scaling of gate oxides [1]. This trend reached a critical milestone at the 0.25 μm technology feature size, where oxide gate thickness (Tox ~ 6 nm) became comparable to the characteristic hole tunneling length [2]. The gate thickness was further scaled to ~2 nm at the 90 nm technology node, insuring negligible gate oxide-trapped charge build-up, and therefore virtually eliminating the TID issue in SiO_2-based gate oxides. However, along these improvements emerged concerns about the TID response of shallow trench isolation (STI) oxides enclosing the active MOS transistor.

Their ability to build-up net positive oxide-trapped charge, just like thick gate oxides did in older CMOS technologies, can potentially lead to the creation of parasitic leakage current paths, severely increasing an IC's standby current, and more critically, affecting its reliable operation.

It is with these concerns in mind that we investigate the TID susceptibility of high-density SRAMs fabricated in a 90 nm commercial bulk CMOS technology. SRAMs are ideal worst-case benchmark vehicles due to their particular sensitivity to the rising STI issue: they are designed with "special SRAM rule" wavers, heavily favoring chip density for increased performance. However, the shrinking of minimum spacing rules can potentially favor the formation of leakage paths between STI-isolated regions, leading to drastic leakage current increase. Thus, any TID-induced charge effects along a STI sidewall/base are also prone to exhibit an exacerbated impact on SRAM operations, when compared to ICs designed in standard "logic rules".

In this work, we show that TID-induced intra/inter-device leakage paths between isolated diffusions result in a steep standby current increase in 90 nm SRAM circuits, occurring only past 300 krad(Si). Additionally, the parasitic leakage currents manage to perturb the intricate current balances determining the SRAM's timing and sensing for Read/Write operations to the point of critical functional failure ~ 1 Mrad(Si). Furthermore, we also show that 90 nm commercial-density SRAMs are very responsive to temperature annealing treatments: they are able to regain pre-radiation nominal characteristics within few hours of high-temperature anneal, after having been irradiated to a TID level of 2 Mrad(Si) and having exhibited at that point a complete loss of functionality as well as orders of magnitude increase in leakage current.

In what follows, we introduce the devices under-test (DUTs) and the experimental setup used. Then we first present results pertinent to the TID response of 90 nm commercial-density SRAMs, with independent monitoring of Core circuit and IO leakage currents. We follow-up by investigating the annealing response of SRAMs for 3 temperature cases (24°C, 100°C and 150°C), and finally discuss the shifts observed in their radiation response across repeated exposure/annealing cycles.

Manuscript submitted September 10 , 2008. This work was supported by the Defense Advanced Research Projects Agency (DARPA) Microsystems Technology Office under award No. N66001-04-1-8914. Any opinions, findings, and conclusions or recommendations expressed in this work are those of the authors and do not necessarily reflect the views of DARPA/MTO or the U.S. Government. The U.S. Government is authorized to reproduce and distribute reprints for Governmental purposes notwithstanding any copyright notation that may appear hereon.

Y. Boulghassoul, M. Bajura, S. Stansberry, J. Draper, R. Naseer and J. Sondeen are with the University of Southern California Viterbi School of Engineering Information Sciences Institute, Marina Del Rey, CA 90292 USA. (phone 703-812-3715; fax 703-812-3712; emails: yboulgh@east.isi.edu, mbajura@isi.edu, sstans@east.isi.edu, draper@isi.edu, naseer@isi.edu, and sondeen@isi.edu).

II. TEST DEVICES AND EXPERIMENTAL SETUP DESCRIPTION

The SRAM test chips presented in this effort were designed and fabricated in two process variations of the same 90 nm bulk CMOS technology: a low power and a high performance one that we shall name LP and SF respectively. Each chip incorporated two SRAM devices: 1) a 64kb unhardened fully COTS (Commercial Off-The-Shelf) SRAM, to be used as the baseline benchmark for the radiation sensitivity assessment in each of the LP and SF processes, and 2) a hardened-by-design SRAM, with techniques for TID mitigation (annular gate transistors) in the peripheral logic (i.e. row/column decoders, sensing amplifiers, timing control structures and ECCs), *but still using a COTS memory array structure* to preserve maximum density: in all cases, the basic memory element was always a dense foundry-provided 6T SRAM cell, implemented with SRAM design rule waivers.

The TID tests were performed at the Boeing Radiation Effects Laboratory GammaCell 220E ^{60}Co irradiator. All tests were performed under bias at a dose rate of 200 rad(Si)/s and followed MIL-STD-883E, Method 1019.6 specifications: DUT temperature during irradiation was kept below 30°C and measurement time between two successive irradiation steps was ~15 mins. The structural and electronic support was provided by a Spartan-3 FPGA-based Xilinx Avnet tester developed in-house. The tester controlled the bit patterns loaded on the SRAMs during and after exposures (checkerboard and checkerboard_bar respectively), and executed the various Read/Write commands defined by the testing algorithms. After each exposure step, the DUTs were monitored for increases in leakage current as well as for loss of functionality and corruption of stored data values. The sample size for the experiments consisted of 4 LP and 4 SF chips, each one having a baseline and a hardened SRAM version, for a total of 16 DUTs.

For completeness of information, we will mention that the LP and SF hardened SRAMs also incorporate error correcting circuitry with incremented strength (1-bit Hamming ECC for LP, 2-bit BCH ECC for SF), justifying the augmented sizes of the hardened SRAMs: 88kb for LP and 128kb for SF. To facilitate comparisons of TID responses between various DUTs, all leakage current results for SRAM Cores are presented normalized per bit. Results for the TID response of IO circuitry are presented as measured.

III. TID DAMAGE IN 90 NM LP AND SF SRAMS

In Figs. 1 and 2, we present the evolution of the LP and SF SRAM leakage currents as a function of TID exposure levels, for the SRAM Core (memory array + peripheral logic) and IO circuitry respectively. During irradiation and post-rad measurements, the LP SRAM Core was biased at Vdd=1.2V while the SF SRAM Core was biased at Vdd=1V. The IO circuitry for both LF and SF SRAMS was consistently biased at Vdd=2.5V.

A. TID Impact on Core SRAM Leakage Current

Fig. 1 results show that the standby current of both LP and SF SRAMs stays well behaved (<2X) up to 300 krad. However, it starts increasing steeply past that mark, where both leakage currents ramp up with near identical slopes of 0.3 nA/bit/krad(Si). By the time the 1 Mrad irradiation step is reached, the LP standby current increased ~ 500X while the SF increased about 35X (having started 30X higher than LP). At higher TID exposures, both leakage currents slowly saturate to reach 0.2 μA/bit at 2 Mrad(Si).

When presenting the Core leakage current results, we did not make a distinction between the baseline and the hardened version of LP or SF SRAMs for the following reason: once normalized to the size of the respective memory array, leakage current plots from baseline SRAMs and their corresponding hardened counterparts overlapped perfectly. This indicates that the standby current response of 90 nm LP and SF SRAM Cores is dominated by the leakage induced in the dense memory array, as it swamps any TID hardness gained by implementing annular transistor designs in the peripheral logic.

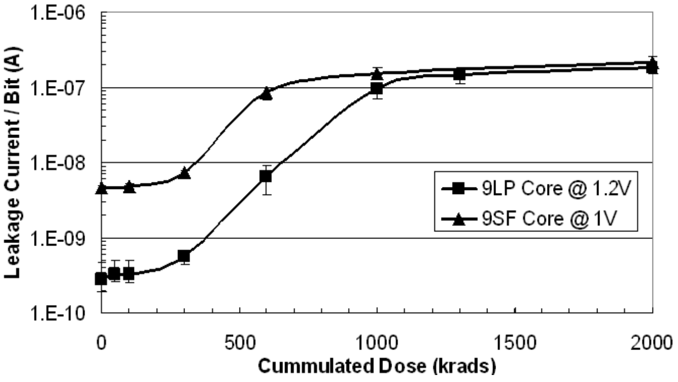

Fig. 1. TID responses of 90 nm commercial-density SRAM Cores, for two process variation as a function of cumulated dose: low power (LP) and high performance (SF).

B. TID Impact on IO SRAM Leakage Current

The difference in TID response between SRAM baseline and hardened IOs contrasts sharply with the previous SRAM Core results. While applying selective TID hardening techniques to the peripheral logic did not seem to impact the SRAMs Core leakage, we see here a drastically improved response from any IO circuitry that incorporated annular designs. Fig. 2 shows an immediate onset of leakage current increase for unhardened IOs, reaching ~1000X at 300krad and 10000X at 2Mrad, while hardened IOs did not respond to TID across the entire exposure range (within experimental detection capabilities).

C. TID Impact of SRAM Functionality

In addition to various leakage current increases in Cores and unhardened IOs, all SRAM DUTs sustained a catastrophic functional failure below the strategic requirement of 2Mrad(Si). All LP SRAMs exhibited a condition where they were no longer responsive to Read/Write commands between the 1 to 1.3 Mrad(Si) irradiation steps. A similar critical failure was observed in all SF SRAMs as well, although it happened between the 600 krad to 1 Mrad(Si) step. This seems to indicate a leakage current "threshold" ~ 0.1μA/bit past which the reliability of the SRAMs becomes critically compromised.

The functionality failure in LP and SF SRAMs occurred regardless of the use of hardened IOs or the incorporation of selective TID hardening techniques in the peripheral circuitry, leaving the SRAM memory array (that is unhardened in all cases) as sole potential culprit for the observed condition. This hypothesis is furthermore validated by the increased detection of "burned-in" bit patterns at the last irradiation step prior to functional failure: power-cycled SRAMs exhibited a preferential bit pattern at first start-up (the one held in memory during irradiation) instead of a random memory bit arrangement. At that point, the exposed memory would require several consecutive Write commands to properly acquire a bit pattern reverse to the one stored during irradiation (in our case checkerboard_bar).

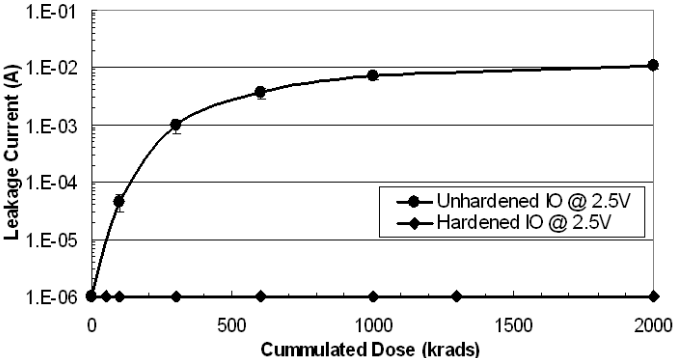

Fig. 2. TID responses of 90 nm commercial-density SRAM IOs , for two design variation as a function of cumulated dose: unhardened IO (baseline) and TID hardened IO.

From the results presented in this sections, we can conclude that 90 nm high-density SRAMs designed in this commercial technology seem intrinsically well suited for space applications with lifetime TID exposures not exceeding 300krad(Si). However, certain specific design precautions have to be considered: although the use of TID hardening techniques in SRAM peripheral logic did not seem worth the incurred penalties (i.e. area and speed), it showed to be critical for insuring well behaved IO leakage characteristics. With gate oxides ~3X thicker than regular logic and higher gate biases, IO FETs exhibit a high sensitivity to TID damage. Nonetheless, this sensitivity can be totally mitigated by the use of annular gate designs, with negligible added area and speed penalties (thanks to the IO's already large original dimensions).

IV. ANNEALING RESPONSE OF 90NM SRAMS AS FUNCTION OF TEMPERATURE

All temperature anneals were performed on unbiased DUTs. Although it is a departure from standard annealing test practices, unbiased anneals provide a worst-case response scenario, as it is well established that operational-bias anneals favor the neutralization of oxide-trapped charge and reduce time-to-recovery at a given temperature [4].

A. *Room Temperature Annealing*

Recovery from TID damage at room temperature (24°C) is very slow (Figs. 3a and 3b) for both Core and IO leakage currents. Although all the 9LP SRAM chips regained full functionality after 7 days of unbiased anneal, after having exhibited catastrophic failure at 2Mrad, the leakage current of the Cores was still 50X higher than pre-rad conditions after 140 days. In the SF case, only half of the chips regained functionality after 7 days. However, all chips were again functional at the 140-day measurement mark, with a Core standby current noticeably below the critical leakage current "threshold" of 0.1μA/bit (~8X of pre-rad conditions). The unhardened IO recovery was even less pronounced as the leakage current was barely reduced by 2X after 140days from its maximum degradation level at 2 Mrad, with most of it happening during the first 7 days of room temperature annealing. Finally, as expected, the hardened IO remained unperturbed. Because of this, we will only mention the leakage response of unhardened IOs in the rest of the paper.

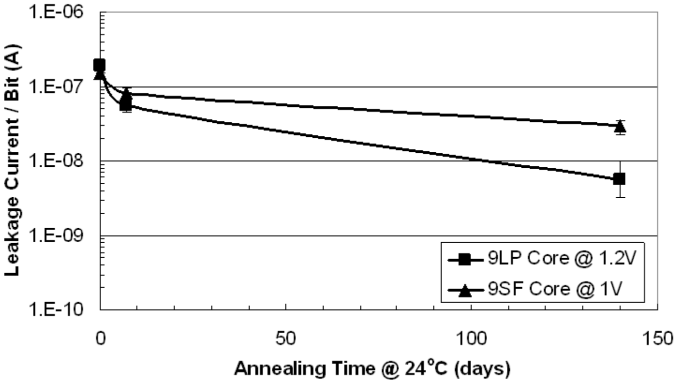

Fig. 3a. Annealing response of 90nm LP and SF SRAM Cores under room temperature (24°C) unbiased anneal.

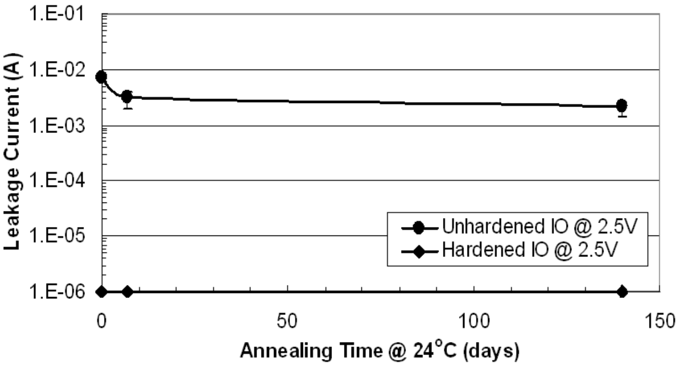

Fig. 3b. Annealing response of 90nm SRAM IOs under room temperature (24°C) unbiased anneal, for unhardened (baseline) and TID hardened design variations.

B. Annealing at 100^{o}C and 150^{o}C

In what follows, we illustrate the typical Core and IO leakage current responses of the 9LP and 9SF DUTs, for the 100°C and 150°C annealing temperature conditions. The authors would like to point out that some annealing data start slightly below the maximum leakage levels previously recorded (ref. Figs. 1 and 2 @ 2 Mrad(Si)), due to a brief uncontrolled anneal that took place during travel between testing facilities.

We can see in Fig. 4a that annealing the DUTs at 100°C manages to bring the TID-induced leakage currents in 9LP Core SRAMs within 3X of their pre-rad levels after 100 hours, and reaches the 2X pre-rad mark at ~ 200 hours. Annealing the 9SF SRAM Core currents at 100°C is noticeably more effective as they reach near pre-rad condition in little over 50 hours of unbiased anneal (Fig. 4ab). However, this annealing temperature is ineffective in inducing any major recovery in the DUTs' unhardened IOs. Fig. 4c shows that their recovery after 200 hours of 100^{o}C anneal is comparable to a room temperature anneal for the same duration (ref. Fig.3).

Most importantly, Figs. 4a, 4b and 4c show that annealing at 150°C yields far more satisfactory results for both 9LP and 9SF SRAM Cores, and for unhardened IOs as well. All chips achieved nominal functionality and Core leakage conditions in less than 5 hours. Unhardened IOs annealed slower, but recovered by ~1000X within the first 50 hours, past which the leakage reduction was at near stagnation ~ 10X above pre-rad.

Although such high annealing temperature might be first deemed deleterious to the long term reliability of SRAMs (or any other circuit), one should keep in mind that it is still fairly comparable to the reliability and qualification burn-in test for this 90 nm commercial bulk CMOS technology (140°C). Additionally, since the parts were annealed unbiased, the impact of thermally enhanced phenomena like electro-migration and hot-carrier damage (both critical to the reliability of modern electronics) is likely to be much lessened by the absence of bias-induced electric fields. Within our limited sample size of 16 DUTs, we did not observe any high temperature annealing-induced IC failure.

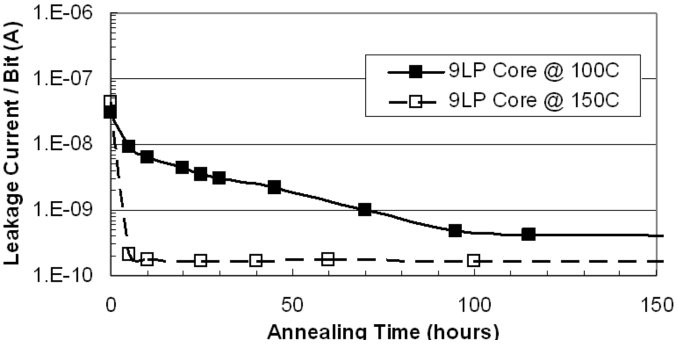

Fig. 4a. Annealing response of 90nm LP SRAMs under 100^{o}C and 150^{o}C unbiased anneal

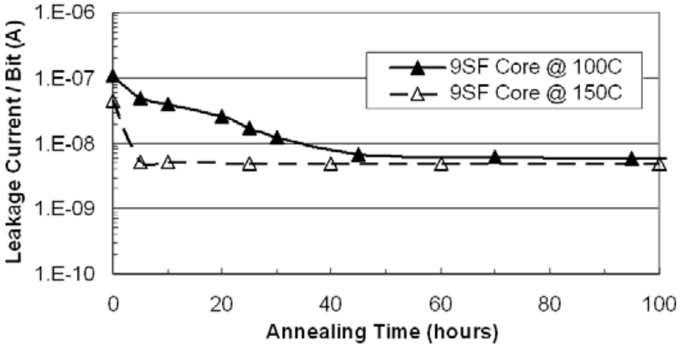

Fig. 4b. Annealing response of 90nm SF SRAMs under 100^{o}C and 150^{o}C unbiased anneal.

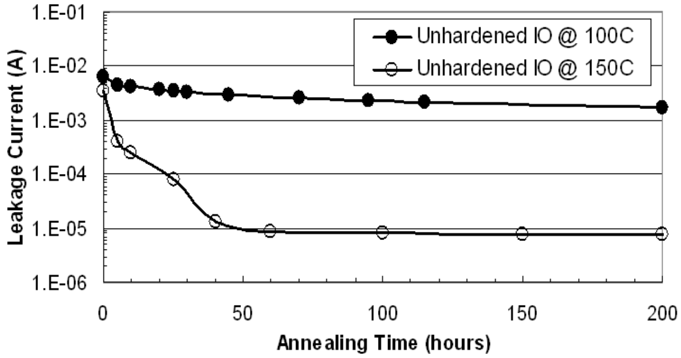

Fig. 4c. Annealing response of unhardened IOs under 100^{o}C and 150^{o}C unbiased anneal.

V. IMPACT OF ANNEALING CYCLES ON THE FUNCTIONALITY OF 90 NM SRAMS

In view of the near-complete recovery from TID damage exhibited by the DUTs, following a brief unbiased high-temperature annealing step, we are prompted to look into the sustainability of this behavior for possible applicability to system-level TID mitigation methods. In what follows, we investigate the impact of repeated exposures on SRAMs' reliability as well as how annealing characteristics are carried over across consecutive annealing cycles.

Figs. 5a and 5b illustrate the respective responses of fresh 9LP and 9SF SRAM test chips. These chips were successively:

1- Exposed to TID radiation past their critical functionality failure threshold up to 2 Mrad(Si)
2- Annealed at 150^{o}C to ensure recovery to pre-rad leakage levels
3- Exposed a second time up to 2 Mrad (Si), in experimental conditions identical to the first exposure.
4- Annealed again at 150^{o}C to attempt recovery to pre-rad leakage levels
5- Exposed a third and final time up to 2 Mrad (Si), in experimental conditions identical to the first exposure.

As Figs. 5a, 5b and 5c curves show, re-exposed SRAMs exhibit singular shifts in their current degradation characteristics.

During the second exposure cycle, all chip Core currents presented an accelerated degradation of standby current, with the onset of severe degradation (>2X pre-rad) starting now at ~200 krad(Si). Additionally, both 9LP and 9SF SRAM Core TID responses showed an early inflexion (~500 krad(Si)) and saturated at lower leakage current amplitudes (Figs. 5a and 5b respectively). But most importantly, *NO functional failures were detected in any chips up to 2 Mrad(Si)*. This behavior contrasts sharply with the observations reported earlier, where all DUTs exhibited a functional failure half-way during their first exposure. Similar shifts in current characteristics were also observed in unhardened IOs (Fig. 5c), although the 150°C anneal after the first exposure was unable to lower the TID damage to pre-rad levels.

The third exposure continued the shifts in TID responses initiated by the previous cycle, with the exception of the "TID onset level" that seemed to have stayed constant or slightly reversed: the leakage current slope past onset has further degraded with an even softer change in inflexion, and the leakage current at 2Mrad(Si) has again saturated at a lower maximum. But once again, *NO functional failures were detected during the experiment*. Finally, shifts in the unhardened IOs were much less pronounced as only the decrease in final saturation current could be clearly observed.

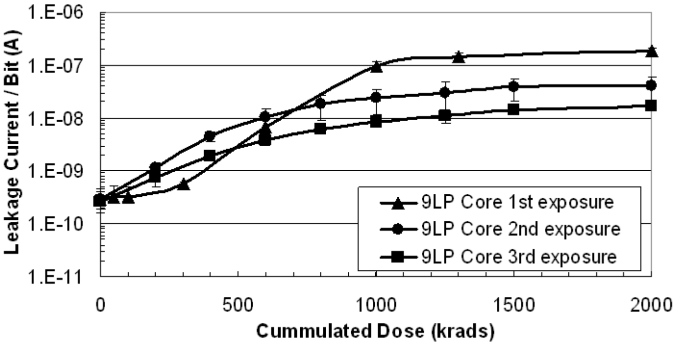

Fig. 5a. TID response of 90nm LP SRAM Cores for a second and third exposure cycle, each preceded by a high temperature annealing step (150°C) to regain pre-rad leakage levels.

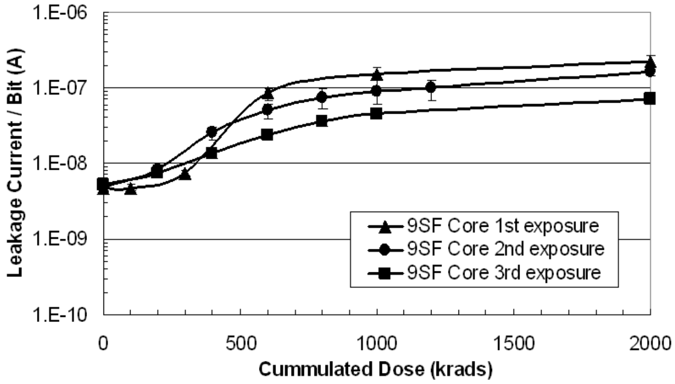

Fig. 5b. TID response of 90nm SF SRAM Cores for a second and third exposure cycle, each preceded by a high temperature annealing step (150°C) to regain pre-rad leakage levels.

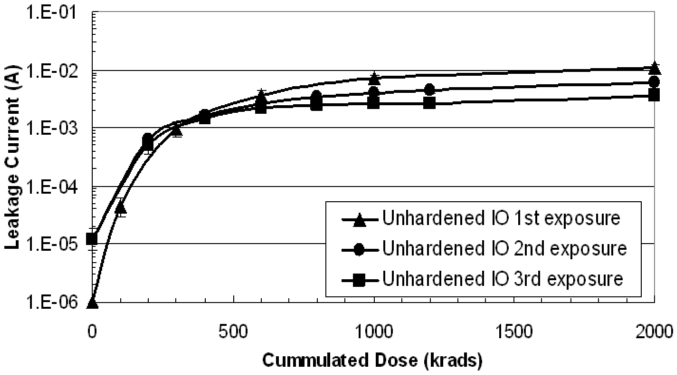

Fig. 5c. TID response of 90nm unhardened IOs for a second and third exposure cycle, each preceded by a high temperature annealing step (150°C) to regain near-pre-rad leakage levels.

VI. DISCUSSION

To explain the various shifts in leakage characteristics as well as the unexpected improvement in SRAM functionality after a high-temperature treatment, we suggest that the main mechanism at play is positive threshold voltage shift in parasitic NMOS transistors present at the thin-to-thick gate oxide transition and across the thick field oxides, due to interface trap build-up. While each high-temperature anneal drastically reduces the positive oxide trapped charge density (Not) induced during the previous exposure, it does not affect the negative interface trapped charge density (Nit) that was also created during the same irradiation step. Therefore, for each successive irradiation, the Not in the STI slowly increases by adding to the remaining Not from the previous anneal, while the Nit at the STI interface compounds with the Nit that the previous anneal has left intact.

This hypothesis was first considered when we compared the TID response of freshly irradiated SRAMs (first exposure) to SRAMs that did undergo a high-temperature treatment (burn-in at 150°C for 50 hours) before their first exposure. The results are depicted in Fig.6, where we found that pre-irradiation temperature stress had no effect whatsoever on the DUT's TID response or survivability: the leakage current characteristics of the temperature-stressed 9LP and 9SF DUTs overlapped very closely with the ones of "fresh" DUTs and all chips failed at the same irradiation step described in section 2.C. This suggested that the improvement in reliability observed in SRAMs during their second exposure was a consequence of mechanisms triggered only after the first post-rad high-temperature annealing.

Additionally, the response of Not and Nit to temperature has very different dynamics [5]. While oxide trapped charge builds-up promptly during exposure and gradually anneals with increasing temperature, interface trapped charge actually builds up between 25°C and 150°C (requiring up to 300°C to start showing some noticeable decrease), thus leading to the phenomena know as "rebound" in thick gate oxides [4]. Although our annealing steps were performed unbiased, we see a reduction in leakage currents (especially between cycle 2 and cycle 3) that corroborates a start of rebound effect in the parasitic transistors: at each new radiation/anneal cycle, they progressively become less “leaky” thanks to the accumulation of interface traps that slowly turn the parasitic channels “more OFF”.

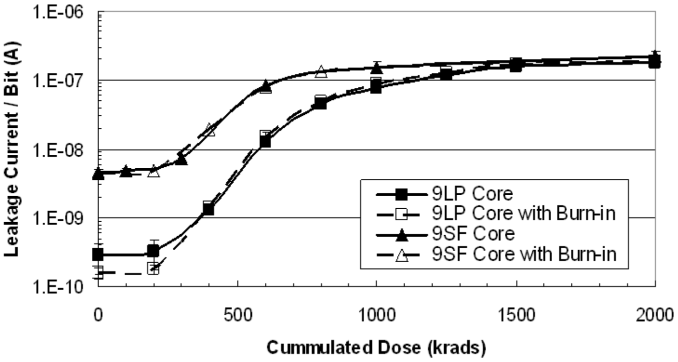

Fig. 6. Comparison between the TID response of fresh 90nm SRAM Core with identical SRAMs that were submitted to a burn-in test (150^{o}C for 50 hours) prior to first irradiation.

Finally, activation energy (Ae) extrapolations from Figs. 4a and 4b seem to further agree with our hypothesis of interface trap build-up in the STI walls, as we obtained an Ae of ~0.85eV and ~0.7eV for the 9LP and 9SF Core SRAM respective recoveries (Ae of interface trap creation ~ 0.8eV [6]). However, the authors are cautions about these last results, as extracting the Ea of a “transistor-level” mechanism through multiple layers of complex circuitry such as the investigated SRAMs can induce a fair amount of error. A collaborative effort, joining experimental work and TCAD simulations on field oxide transistors, is currently under way to further accurately investigate the uncovered phenomena.

VII. SUMMARY AND CONCLUSION

In this paper, we first present the TID damage and annealing responses of high-density SRAMs fabricated in two variations (low power and high performance) of a 90 nm commercial bulk CMOS technology. The monitoring of SRAM standby currents and functional failure thresholds reveal that this 90nm technology continues the trend of improving intrinsic TID hardness with scaling: it operated flawlessly with less than 2X increase in standby current up to 300 krad(Si), making it potentially appropriate for most space applications if special TID hardening considerations are applied to the IO devices. Additionally, we also show that the SRAMs suffer from several orders of magnitude increase in leakage current past 1 Mrad(Si) of exposure with recorded critical functionality failures, thus failing the 2 Mrad(Si) strategic TID resilience requirement.

However, post-radiation annealing tests show that the 90nm commercial technology is very responsive to temperature treatments: following a TID exposure up to 2 Mrad, all SRAM chips 1) regained full functionality and recovered within 3X of their pre-rad leakage current levels in less than 100 hours at 100^{o}C, and 2) all chips recovered to pre-rad levels after 5 hours at 150^{o}C, also with full functionality. Additional exposure/anneal cycles showed a slight decrease in SRAM resilience to TID with an earlier leakage onset, but it also revealed a drastic improvement in SRAM survivability: all test chips that did undergo at least one exposure/anneal cycle stayed fully functional up to 2Mrad(Si).

The mechanism behind the SRAM’s survivability improvements is suggested to be interface trapped charge build-up along the STI walls (sidewalls and trench base), inducing a positive threshold voltage shift in the parasitic “edge” and field oxide NMOS transistors, and resulting in improved inter/intra device leakage isolation.

ACKNOWLEDGMENT

The authors would like to thank Dr. M. Fritze at DARPA and Dr. C. Hanson at SPAWAR for supporting this work; and the staff at the Boeing Research Laboratory for helping with the experimental facilities use.

REFERENCES

[1] J. V. Osborn, D. C. Mayer, R. C. Lacoe and G. Yabiku, “Total Dose Hardness of Three Commercial CMOS Microelectronics Foundries,” IEEE Trans. on Nucl. Sci., vol. 45, no. 3, pp. 1458-1463, Jun. 1998.

[2] G. Anelli, M. Campbell, C. Dachs, F. Faccio, A. Giraldo, E. Heijne, P. Jarron, A. Marchioro, E. Noah, A. Paccagnelle, P. M. Signe, W. Snoeys and K. Vleugels, “Total Dose Behavior of Submicron and Deep Submicron CMOS Technologies,” Proc. 3rd Workshop on Elec. For LHC Experiments, pp. 139-143, Sept. 97 (CERN/LHCC/97-60, 21 Oct, 1997)

[3] M. R. Shaneyfelt, P.E. Dodd, B. L. Draper and R. S. Flores, “Challenges in Hardening Technologies Using Shallow-Trench Isolation,” IEEE Trans. on Nucl. Sci., vol. 45, pp. 2585-2592, 1998.

[4] J. R. Schwank, P. S. Winokur, P. J. McWhorter, F. W. Sexton, P. V. Dressendorfer and D. C. Turpin, “Physical Mechanisms Contributing to Device Rebound,” IEEE Trans. on Nucl. Sci., vol. 31, pp. 1434-1438, 1984.

[5] S. M. Sze, Physics of Semiconductor Devices, Second Edition (New York: John Wiley & Sons, 1981).

[6] J. R. Schwank, D. M. Fleetwood, M. R. Shaneyfelt, P. S. Winokur, C. L. Axness, and L. C. Riewe, “Latent Interface-trap Buildup and its Implications for Hardness Assurance,” IEEE Trans. on Nucl. Sci., vol. 39, pp. 1953-1963, 1992.