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A Novel Model for On-chip Heat Dissipation

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Abstract

This paper presents an analytical model for on-chip heat dissipation in VLSI design. A chip and its test configuration also are developed to verify modeling results. The model and chip are representative of general IC packages. Our research shows that circuit location on a chip determines its default offset temperature and heat transport properties, which must be considered for accurate prediction of junction temperature and electro-thermal analysis. The model yields insights about on-chip heat dissipation, which are very useful for mixed-signal VLSI designs and circuit reliability analysis.

1. Introduction

On-chip thermal distribution is an important factor in high-speed VLSI design[1], SOI Circuits[2] and MCM (Multi Chip Module) systems. Much research has focused on the predictions of junction temperature and power generation in circuits[3, 4]. Recent approaches have combined thermal transport properties to get more precise predictions[5, 6]. Meshing[7], finite element analysis and thermal circuits[8] are popular methods to simulate thermal transport properties. However, meshing and thermal circuits introduce some difficulties. For instance, different meshing approaches or thermal circuit models generate different results for the same circuit, often differing by as much as two orders of magnitude in thermal transport properties. Furthermore, these methods tend to produce intricate mathematics, and the solutions are often elusive.

In this paper, we present an analytical model based on general heat source setup and heat transfer assumptions. Applying differential equation theories, we achieve a set of continuous equations, which describe the thermal transport properties on each point of a die. The model provides clean, simple analytical solutions of heat dissipation conditions, which yield the offset temperature for junction-temperature estimation and on-chip thermal distribution predictions. In Section 2, we describe assumptions and justification for the assumptions, as well as the derivation and results.

In Section 3, we present a chip and its testing configuration[9]. The chip was designed to verify the models we describe in Section 2. Using a specialized floor plan and circuit modules, we are able to simplify the thermal transport properties to verify the models. The configuration for calibration and testing are also described.

Along with the design and configuration, we present the measured results in Section 4. Both theoretical and measured results are discussed here. The utilities of the results are discussed, and potential improvements are also addressed.

2. Model Development

The goal of our model is to develop a set of equations to calculate the temperature distribution regarding geometry and time. We define a chip with a periodic heat source applied in the center of the upper face. The heat transfer on fives sides of the chip (upper side and surrounding four sides) are modeled as adiabatic processes, while the bottom side attached to the package is modeled as an isothermal process. Therefore, heat will dissipate from the center to the package. This assumption is based on the packaging style of most die. The five adiabatic sides have a die to air interface, which has negligible heat transfer compared to the die-package interface. The bottom side is isothermal, because the package is assumed adequate for dissipating heat immediately from the die to the outside environment.

Using the above assumptions as the boundary conditions, and solving using partial differential equation theory, we get the following results. Define the temperature function as $u(x,y,z,t)$ *with* $x,y,z\in\Gamma$, $t>0$

$$\Gamma=\left\{(x,y,z)\middle|-\frac{L}{2}\le x\le\frac{L}{2},-\frac{L}{2}\le y\le\frac{L}{2},-w\le z\le 0\right\}$$

where t is time, Γ is the geometry of the die, x,y,z represent the coordinates, L is the length of the edge of the die, and w is the thickness of the wafer. Assume there is a unit heat source placed at the point $(0,0,0)$ at $t=0$. We want to know the temperature distribution of Γ at any given moment for $t>0$. The boundary condition is prescribed by a Neumann problem (adiabatic) on 5 faces of Γ other than the bottom face, and a Dirichlet (isothermal) problem on the bottom face. From partial differential equation theory, we know this problem has a unique solution for u.

$$u(x,y,z,t)=8\cdot\left[\sum_{k=0}^{\infty}e^{\frac{-4k^2\pi^2t\gamma}{L^2}}\cos(\frac{2k\pi x}{L})\right]\times\left[\sum_{k=0}^{\infty}e^{\frac{-4k^2\pi^2t\gamma}{L^2}}\cos(\frac{2k\pi y}{L})\right]\times\left[\sum_{k=0}^{\infty}e^{\frac{-(2k+1)^2\pi^2t\gamma}{4w^2}}\cos(\frac{(2k+1)\pi z}{2w})\right] \qquad (1)$$

where $\gamma=\frac{K}{\rho\times C_p}$, *K* is the thermal conductivity, ρ is density, and *Cp* is the heat capacity of silicon.

$$u_\infty(x,y,z,t)=\sum_{\tau=0}^{\infty}u(x,y,z,t+\frac{\tau}{f})$$, where $0<t<\tau$, f is the frequency (2)

$$u(x,y,z,t)=\sum_{\tau=0}^{\infty}8\cdot\left[\sum_{k=0}^{\infty}e^{\frac{-4k^2\pi^2(t+\frac{\tau}{f})\gamma}{L^2}}\cos(\frac{2k\pi x}{L})\right]\times\left[\sum_{k=0}^{\infty}e^{\frac{-4k^2\pi^2(t+\frac{\tau}{f})\gamma}{L^2}}\cos(\frac{2k\pi y}{L})\right]\times\left[\sum_{k=0}^{\infty}e^{\frac{-(2k+1)^2\pi^2(t+\frac{\tau}{f})\gamma}{4w^2}}\cos(\frac{(2k+1)\pi z}{2w})\right] \qquad (3)$$

Let's assume $u(x,y,z,t) = u_1(x,t)\cdot u_2(y,t)\cdot u_3(z,t)$. Then from Libniz rule, we know

$$\begin{aligned}\left(\Delta-\frac{\partial}{\partial t}\right)\cdot u(x,y,t) &= \left[\left(\Delta_x-\frac{\partial}{\partial t}\right)\cdot u_1(x,t)\right]\cdot u_2(y,t)\cdot u_3(z,t)\\ &+u_1(x,t)\cdot\left[\left(\Delta_y-\frac{\partial}{\partial t}\right)\cdot u_2(y,t)\right]\cdot u_3(z,t)\\ &+u_1(x,t)\cdot u_2(y,t)\cdot\left[\left(\Delta_z-\frac{\partial}{\partial t}\right)\cdot u_3(z,t)\right]\end{aligned}$$

Therefore if we can solve $u_1(x,t)$, $u_2(y,t)$ *and* $u_3(z,t)$ satisfying the prescribed boundary conditions, then we can solve *u*. Each function has its own boundary condition and solution. Therefore, we obtain the thermal distribution function given in Equation 1.

Finally, we compute the case when there are unit heats added to the origin periodically. The temperature distribution function, $u_\infty(x,y,z,t)$ is a periodic function after infinite unit heat sources are added. We obtain the thermal distribution function given in Equation 2.

We then combine Equation 1 and 2 to form Equation 3, which can be used to predict spatial and temporal temperature differences.

3. Validation of Model: Design and Configuration

The above model is a simplification of reality. To validate the model, we designed a test chip which matches the assumptions we used in the previous section. The goal of this design is to measure the spatial temperature differences on chip. We use five circuit modules in a spiral floor plan to produce a variety of combinations of heat sources and sensors. Each module contains a pad driver, a poly-silicon resistor, and a diode. The pad driver is used as the heat source. Poly resistors and diodes function as temperature sensors. A picture of the chip layout is shown in Figure 1. The chip was designed and fabricated using a MOSIS 0.5μ process.

Each pad driver is considered a point heat source since it occupies less then 1% of the chip area. Several researchers have verified the accuracy of using diodes and resistors as on-chip temperature sensors[10, 11]. Here we use non-silicide polysilicon resistors, which are provided in the MOSIS 0.5μ process. The diodes and resistors were calibrated using a thermal bath with a thermal chamber and test board. After the calibration, we applied linear regression to get the algebraic expression and lookup table for the temperature sensors.

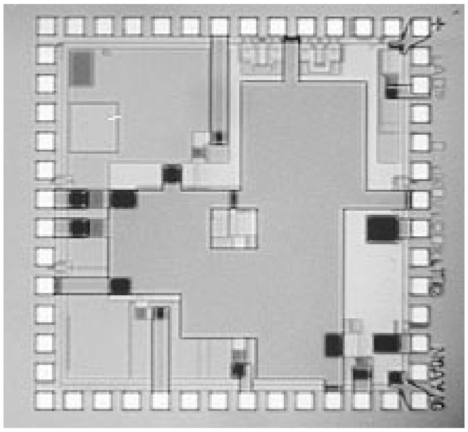

Figure 1. Microscope Picture of the test chip (Circuit modules in a spiral pattern from center to border are labeled PAD1, PAD2, PAD3, PAD4, PAD5, respectively.)

With the above setup and calibration, we measured different combinations of heat sources and temperature sensors. With different combinations of variables, we are able to measure spatial temperature differences. One set of experiments was conducted with a fixed heat source location and varying sensor locations. Another set was conducted with a fixed temperature sensor location and varying heat source locations. Both experiment results and comparison to the model are shown in Section 4.

4. Results

Substituting the geometry, power and frequency of our test chip into the model, we achieved the following temperature plot for the top surface of the die. With appropriate depth of index (*k* = 20 ~ 200), we achieve the reasonable converged values. Suitable values for *k* depend on accuracy and model runtime constraints.

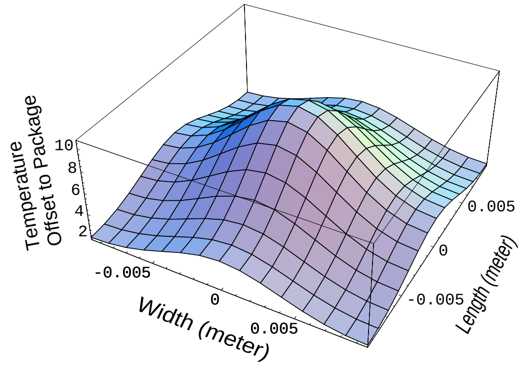

Figure 2. Temperature distribution on die surface, z-axis represents relative temperature difference(°C), x,y represent location on the surface(m), k=20

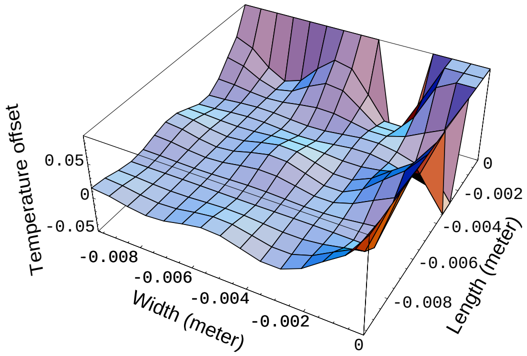

Figure 3. Temperature on a portion of die surface. z-axis represents relative temperature difference(°C), x,y represent location on the surface(m), k=200

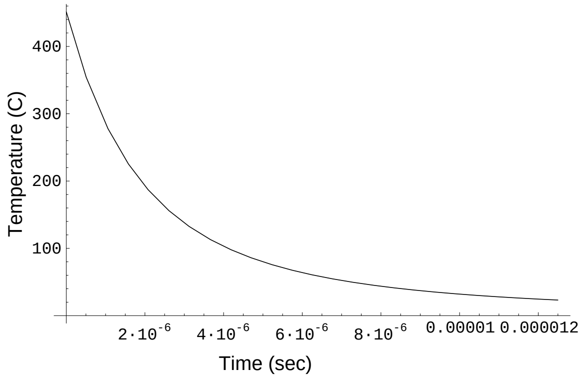

Figure 4. Temporal temperature drops in heat source.

Figure 2 and Figure 3 are plots from Equation 3. Using a small *k*, we can achieve the equilibrium temperature to verify the temperature offset from the measurement. With a larger *k* value, (k=200 for Figure 3), we can examine a smaller portion of the chip in a more detailed fashion. We obtain the ripple style temperature surface which is due to the periodic heat source. The swing on the surface of the chip is 0.02°C where outside the heat source area.

Figure 4 shows the temperature-dropping curve in the heat source location. This result shows a temporal temperature difference of 450°C in transistor junctions. The temporal varying of temperature is significant in limited geometry and cannot be neglected in electro-thermal simulations.

Fixed Heat Source Location Experiments

The spatial temperature differences from our measurement and model are shown in the following table. As shown in the table, the measurements agree within 13% of the model for non-negligible temperature offsets. Figure 5 shows the temperature readings from the measurement.

Module	**#1**	**#2**	**#3**	**#4**	**#5**
Model	9.25	14.58	1.15	0.01	0.00
Measurement	10.52	15.50	2.24	0.00	0.00

Table 1. Comparison of spatial temperature differences from model and measurement.

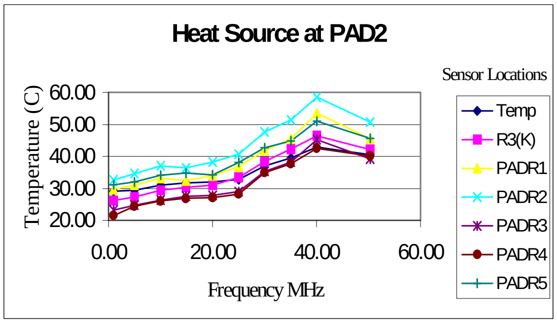

Figure 5. Spatial temperature offset from measurement.

Fixed Sensor Location Experiments

Circuit Frequency	**Heat Source Locations** #2	#3	#4	#5
1.00	29.72	31.90	31.94	29.99
5.00	30.96	31.35	31.39	30.26
10.00	33.18	31.00	31.55	31.74
15.00	32.40	33.26	33.61	30.65
20.00	33.96	31.78	34.81	32.67
30.00	41.89	33.92	34.62	34.39
40.00	53.52	36.37	35.44	32.87
50.00	45.55	39.13	36.02	33.84

Table 2. PAD1 temperature with different heat source

In Table 2, we have measured PAD1's temperature while varying the location of the heat source among PAD2-PAD5. As shown in the data, we achieved a temperature difference of 20.65°C between 0.556W applied at PAD5 versus PAD2. These results show that the spatial temperature offset generated by different locations is significant.

Our theoretical model indicates the center location has a higher temperature of 53.52°C, while the border of the chip has lower temperature. When we apply the same amount of heat in different locations on the chip, we see significant temperature differences on the chip as well as the package.

In Figure 6, we also measured the package temperature while varying the heat source location. There is a 13.40°C difference between a heat source applied at the center versus the border. This result matches our prediction in the model and also confirms that different heat dissipation due to location on the chip is not negligible.

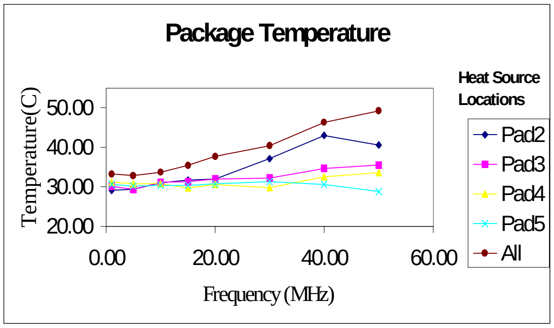

Figure 6. Package temperature.

The results verify the heat dissipation assumptions and the prediction of thermal characteristics of our model. The model is precise, simple and closely matches our measurement results. Our model also predicts the temperature variation in very small amounts of time and show that temporal variations are significant, possibly influencing circuit behavior. A meaningful direction for future work is to attempt to measure this temporal behavior in a test configuration.

5. Conclusion

This paper presents and illustrates the combination of modeling and measurement of thermal distribution for integrated circuits. The quantification of spatial and temporal temperature offsets show that local heat-up cannot be neglected, especially for mixed-signal integrated circuits, multi-chip modules and circuit reliability analysis. A novel model has been derived to predict the temperature differences due to geometry and time. Such measurement results and models provide insight into heat dissipation, which is necessary for transient electro-thermal analysis, junction temperature prediction and on-chip thermal management systems to achieve a more accurate result.

Acknowledgement

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