The Effect of Design Parameters on Single-Event Upset Sensitivity of MOS Current Mode Logic

Mahta Haghi
University of Southern California
Electrical Engineering Department
Los Angeles, CA, USA
mhaghi@usc.edu

Dr. Jeff Draper
University of Southern California
Information Sciences Institute
Marina Del Rey, CA, USA
drpaer@isi.edu

ABSTRACT

In this paper, we describe and discuss the effects of design parameters such as transistor size, output voltage swing and bias current on radiation sensitivity of MOS current mode logic (MCML) type sequential elements that are used in high-speed communication systems. We have implemented latches and flip-flops in 90 nm technology and show how single-event upset can be mitigated just by adjusting particular design factors at the same clock frequency. It is shown that the critical charge needed to upset the logic state of a sequential element increases up to 5 times by increasing the bias current at the cost of more power and up to 2 times by increasing output voltage swing at the cost of more area. The effect of changing operation frequency from 500MHz to 4GHz on single-event upset is also investigated. For frequencies higher than 2 GHz, critical charge improves 1.3 times.

Categories and Subject Descriptors

B.7.1 [**Integrated Circuits**]: Types and design styles- VLSI (Very Large Scale Integration).

General Terms

Design, Performance and Reliability.

Keywords

MOS Current Mode Logic (MCML), Radiation Hardening, Single Event Upset (SEU), Design Parameters

1. INTRODUCTION

Conventional CMOS circuitry typically has advantages of small area, low static power dissipation, high noise margin and availability in standard library cells [1], but in high frequency systems it is not that efficient due to high dynamic power dissipation and coupling of high switching spike noise to power supplies [2]. Also in mixed-signal environments, CMOS causes crosstalk between analog and digital circuitry [3].

Recently, moving to very high speed systems and integrating analog and digital circuitry onto the same die has drawn attention toward MOS Current Mode Logic (MCML), figure 1 [4].

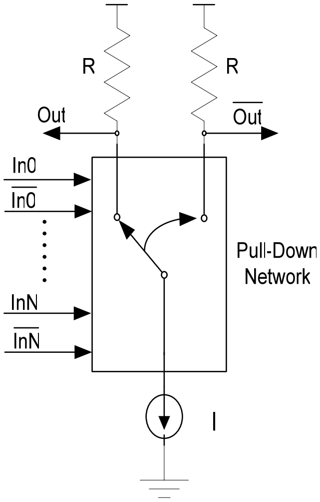

Figure.1 Basic MCML Structure [5]

The MCML structure is completely differential and switches current between two pull-up resistors. The output voltage swing of ΔV=IR is set by adjusting the pull-up resistors for a chosen bias current [5]. Not only is the voltage swing of MCML less than rail-to-rail, but it is also much less than that of CMOS. This makes MCML faster than CMOS and with smaller dynamic power dissipation. The differential structure of MCML also rejects any common-mode noise and distortion.

The reduced output voltage swing decreases crosstalk between analog and digital circuits, hence making MCML a better candidate for mixed-signal applications as well. It draws almost constant current from Vdd, which reduces noise spikes on power supply rails. It is also more flexible in design optimization than CMOS circuits. While CMOS circuits are optimized by changing the device sizes and Vdd voltage, MCML can be optimized by adjusting the output voltage swing, bias current, Vdd and transistor sizes [5]. However, the main disadvantage of MCML is the high constant static power dissipation. Although it may be an issue to take into account for low frequencies, in high frequencies dynamic power becomes the dominant term in power dissipation.

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It has been shown [5, 6] that at high frequencies, the energy-delay product of MCML is significantly less than that of CMOS and is process independent. The energy-delay products for MCML and CMOS are shown in (1) and (2) respectively:

$$ED_{MCML} = \frac{C^2 \times V_{dd} \times \Delta V^2}{I} \qquad (1)$$

$$ED_{CMOS} = 2 \times \frac{C^2}{k} \times \frac{V_{dd}^2}{(V_{dd} - V_t)^{\alpha}} \qquad (2)$$

where C is the load capacitance, $\Delta V = IR$, V_t is the threshold voltage, k and α are process and transistor size dependent parameters.

Therefore MCML is an excellent candidate for high frequency circuits. Considering the increase in the popularity of MCML in both digital and analog circuit applications, we are interested to investigate how these circuits could be used in a radiation-hardening by design approach to build radiation-tolerant circuits. Ions or electro-magnetic radiations that strike a sensitive node in a semiconductor device can cause change of state in memory elements. This unwanted sate change (error) at the output of the effected device, which is a result of free charge created by ionization in or close to a sensitive node of a logic element, is called Single-Event Upset (SEU) [7]. SEU is a problem mainly for memory or sequential elements like latches or flip-flops since it corrupts the state of a cell permanently until reloaded by new data.

In this paper we investigate and discuss the effect of different design parameters such as transistor size, voltage swing and bias current on the SEU tolerance of MCML at different operating frequencies. Section 2 provides some background information. Section 3 presents the implementation details of our approach. Section 4 discusses the analysis of how design parameters affect the performance of our approach, and Section 5 concludes the paper.

2. Critical charge definition and calculation

The minimum amount of charge needed to be collected in a sensitive node to change the state of that node is called critical charge, Q_{crit}, which is an important measure for the SEU sensitivity of a circuit node [8]. Drift and diffusion are the two well-known mechanisms that transport the generated charges to a circuit node. This creates a current pulse that disturbs the node level and leads to a corrupted data bit. Therefore for calculating Q_{crit}, we used a current source to model the current pulse created by the ion strike. We used a double-exponential waveform equation (3) as a model for current source since it results in a conservative Q_{crit} calculation. The rise time (τ_r) of 16 psec and fall time (τ_f) of 161 psec are set in our HSPICE simulation [9].

$$I(t) = \left(\frac{Q}{(\tau_f - \tau_r)}\left[\exp\left(\frac{-t}{\tau_f}\right) - \exp\left(\frac{-t}{\tau_r}\right)\right]\right) \qquad (3)$$

3. Implementation

All circuits are designed in IBM 90 nm technology. The schematic of our design is shown in figure 2. For different clock rates of 0.5, 1, 2 and 4 GHz, the output voltage swing is swept from 300 mV to 500mV. A minimum voltage swing of 300 mV is chosen to ensure signal integrity in the presence of thermal noise and device mismatch [5]. The bias current is swept from 30μA to 500μA while output voltage swing and clock rate are constant. The same procedure is repeated for the other two output voltage swings to observe the effect of output voltage swing. The data frequency is chosen to be half of the clock frequency.

As mentioned above a double-exponential current source is used to model the single-event strike. The current source is placed between the drain of the NMOS in the hold stage and ground level, figure 2. The drains of NMOS transistors in the hold stage are the most sensitive nodes of the MCML latch since any change of the value at these drains changes the output value of the latch.

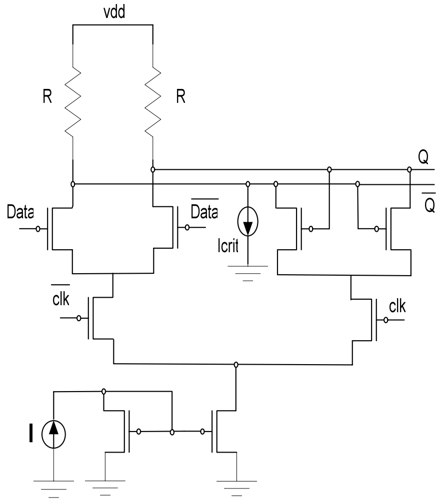

Figure 2. Schematic of MCML Latch, with current source placed between the drain of NMOS in hold stage and ground

We use a current mirror for accurate biasing of the sequential elements. Transistors have been sized according to output voltage. For each output voltage the transistors in the current mirror are sized to be in the saturation region. The lengths of these transistors are set at double the minimum length to increase the output impedance for the current source and to decrease the effects of transistor length mismatch between the biasing and logic circuit [5].

We used poly resistors, as poly has better accuracy compared to nwell and diffusion resistors. Another important reason for using poly resistors over other types is that poly has better immunity to SEU. A Single-Event strike can change an nwell potential and disturb the circuit functionality. The poly resistor is not connected to substrate or nwell; thus, it has a better immunity to disturbances. Area is the trade-off since poly resistors occupy more area compared to nwell resistors.

4. Results and Discussion

In order to distinguish the effect of each parameter on Q_{crit} clearly, we discuss each parameter effect in a different subsection.

4.1 Current Bias effect on Q_{crit}

In order to find Q_{crit}, the charge injected by the double-exponential current source is swept to the point that it flips the output of the flip-flop, as shown in figure 3.

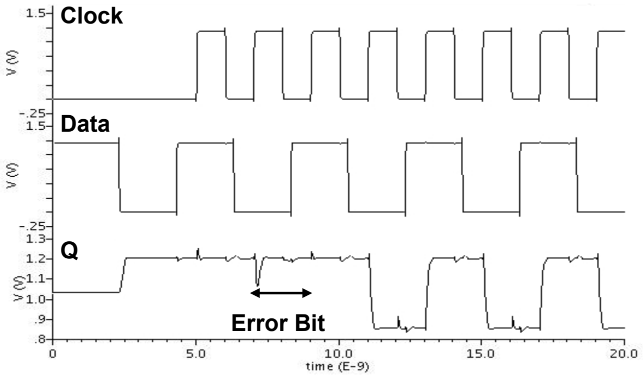

Figure 3. Clock, Data and Output (Q) waveforms of a single-event hit flip-flop.

Figure 4 shows that by increasing the bias current, Q_{crit} increases independent of operating frequency. A larger bias current implies larger transistor sizes, and as a result larger capacitances to hold charge and consequently more immunity to single-event upsets. In table 1, the amount of increase in Q_{crit}, is shown for different output voltage swings at a clock rate of 0.5 GHz when moving from 30 µA to 100µA. It can be seen that the amount of Q_{crit}, increases more than 3 times for output voltage swings of 400 mV and 500 mV. This increase is almost 5 times for an output voltage swing of 300 mV.

Table 1. Q_{crit} Improvement with current bias for different output voltage swing at clock rate of 0.5 GHz

ΔV=IR (mV)	Q_{crit} (fC) at I =30µA	Q_{crit} (fC) at I =100µA	Increase in Q_{crit}
300	0.40	1.94	x4.85
400	0.73	2.67	x3.66
500	0.89	2.83	x3.18

In order to show how much area is scarified to gain more SEU tolerance, we laid out two latches with the resistor and transistor sizes calculated for bias currents of 30 µA and 100 µA (Table 2) at ΔV of 300 mV and a clock rate of 0.5 GHz. The layouts are shown in figure 5. Both layouts occupy about 75 μm^2 of area. This implies that increasing the bias current does not have a significant effect on total layout area. Even though the transistor sizes increase with bias current, pull-up resistor sizes decrease, and this keeps the area almost constant.

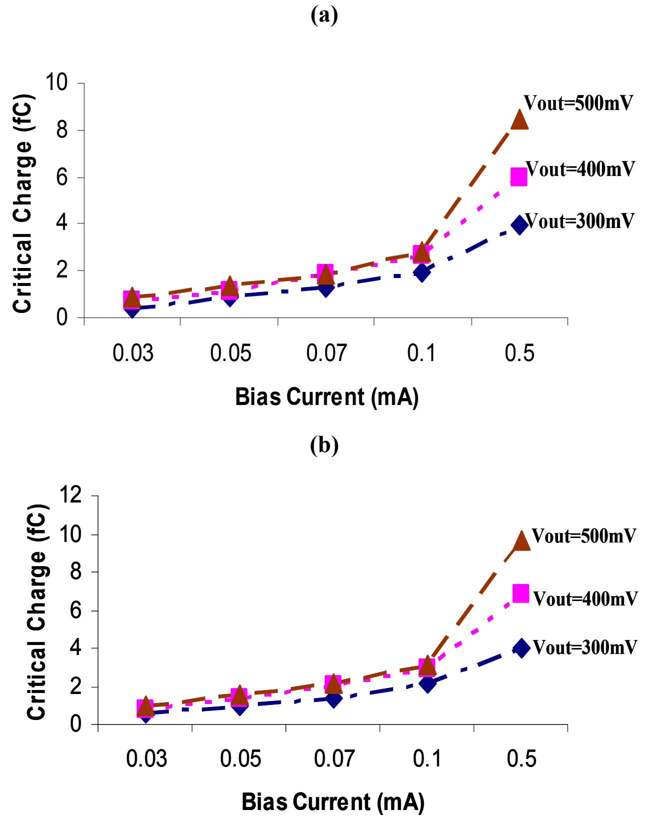

Figure 4. Critical Charge (Q_{crit}) versus Bias Current for different output voltage swings at (a) clock rate of 0.5 GHz, (b) clock rate of 2 GHz.

The important downside of moving to a higher bias current is the power consumption, which increases linearly with bias current. Even though the biasing current of 100 µA is in the tolerable range for MCML, the power budget is the key point that should be considered when designing radiation-hardened MCML.

Table 2. Resistor and transistor sizes for ΔV=300 mV for bias current of 30 and 100 µA at clock rate of 0.5 GHz

I (µA)	Resistance (kΩ)	Pull-down transistor width (µm)	Biasing transistor width (µm)
30	10	0.9	0.6
100	3	4.8	0.6

For a bias current of 500 µA, the increase in Q_{crit} is even more significant, but at a cost of a significant rise in power consumption and area. For example by changing the bias current to 500 µA, Q_{crit} increases by 9.8 times compared to the Q_{crit} at 30 µA, but the exorbitant cost of area and power consumption do not justify this improvement for most applications.

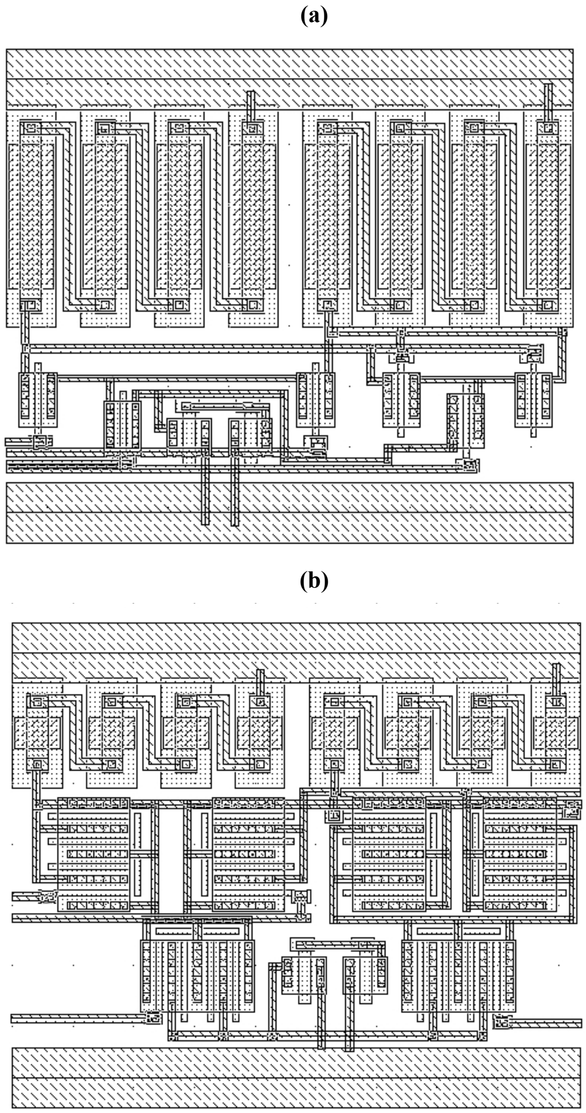

Figure 5. MML Latch lay out for ΔV=300 mV and clock rate=0.5 GHz for (a) I = 30 µA and (b) I = 100 µA

4.2 Output voltage swing effect on Q_{crit}

In this subsection the effect of output voltage swing, ΔV, on Q_{crit} is analyzed. The improvement of SEU tolerance by increasing ΔV is shown in figure 6. Q_{crit} increases as ΔV amplifies due to better margin on the effective voltage ($V_{gs} - V_{th}$) of cross-coupled transistors in the hold stage. This is similar to increasing the noise margin of a circuit. Therefore with higher ΔV at a constant bias current and transistor size, more charge is needed to upset the state of the hold stage.

The improvement in Q_{crit} is shown in table 3, when moving from ΔV= 300 mV to ΔV=500 mV with constant bias current at a clock frequency of 0.5 GHz.

The improvement is more than 1.4 times for bias currents of 50 and 100 µA and 2.2 times for a bias current of 30 µA.

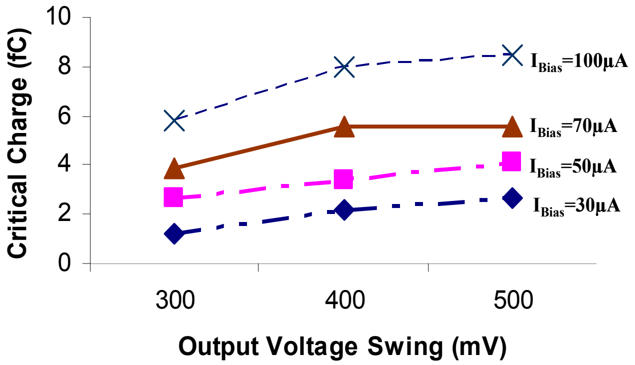

Figure 6. Q_{crit} versus Output Voltage Swing for different Bias Currents at clock rate of 0.5 GHz

Table 3. Q_{crit} Improvement with Output voltage swing for different Bias Currents at clock rate of 0.5 GHz

Bias Current (µA)	Q_{crit} (fC) at ΔV = 300 mV	Q_{crit} (fC) at ΔV = 500 mV	Increase in Q_{crit}
30	0.4	0.89	x2.22
50	0.89	1.37	x1.54
100	1.94	2.83	x1.46

Improving the SEU immunity by changing the ΔV does not increase the power consumption in this case, since the bias current is constant. However area is compromised, since increasing ΔV=IR at constant I increases the size of pull-up resistors (R). As mentioned before and as also can be seen from the layout in figure 5, poly resistors occupy a large percentage of the area in MCML. Thus, if we are limited by power, increasing the ΔV is a promising solution, but area is compromised.

4.3 Clock frequency effect on Q_{crit}

The dependency of Q_{crit} on clock frequency is discussed in this subsection. We simulated MCML at 0.5, 1, 2 and 4 GHz. For clock frequencies of less than 1 GHz, Q_{crit} is independent of clock frequency. At these frequencies, a single-event strike has enough time to create sufficient free charge to upset a node. However, for frequencies of 2 GHz and higher, Q_{crit} increases with clock frequency. The ionization time constants are independent of the clock frequency; therefore, at some point they get larger than the clock period. Thus, a strike needs more energy to create enough charges to upset a node in this short period of time. Therefore, the circuit becomes harder to radiation at high frequencies. Dependency of Q_{crit} to clock frequency is shown in figure 7. Curves for clock frequencies of 0.5 and 1 GHz overlap since at these frequencies Q_{crit} is independent of clock frequency.

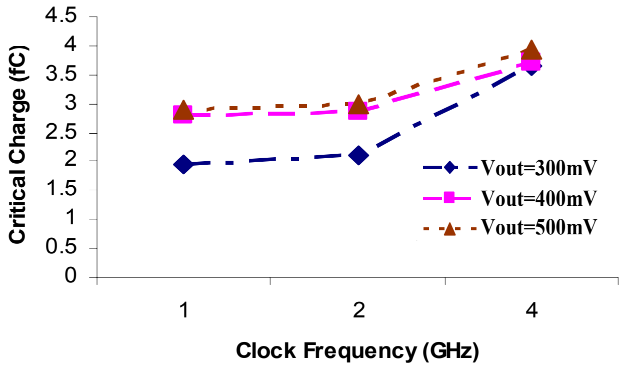

Figure 7. Q_{crit} versus clock frequency for different output voltage swing at Bias current of 100 µV

This improvement in Q_{crit} by increasing the clock frequency is shown in Table 4. Q_{crit} increases about 1.3 times when the frequency is increased from 1 GHz to 4 GHz at a constant output voltage swing of 500 mV.

Table 4. Q_{crit} Improvement with Clock frequency for different Bias Currents at Output voltage swing of 500 mV

Bias Current (µA)	Q_{crit} at Clock frequency=1GHz (fC)	Q_{crit} at Clock frequency=4GHz (fC)	Increase in Q_{crit}
50	1.37	1.78	x1.30
70	1.86	2.51	x1.35
100	2.83	3.92	x1.38

4.4 Speed (delay)

The performance of MCML with respect to clock-to-Q delay was also measured and analyzed. The clock-to-Q delay of MCML has been measured at different bias currents, output voltage swings and clock frequencies. The delays were measured at both rising and falling edges. All the delays are in the order of picoseconds. These delays for the case of 0.5 GHz are shown in table 5. There is little difference in delay values for the differing bias currents shown.

Table 5. Clock to Q delay for different Bias Currents at clock rate of 0.5 GHz and Output voltage swing of 500 mV

Bias Current (µA)	Clock to Q delay for rise edge (ps)	Clock to Q delay for fall edge (ps)	Average delay (ps)
30	70	60	65
50	70	50	60
70	60	40	50
100	70	40	55
500	80	50	65

If we consider the RC model for our delay measurement, then as capacitance (C) goes up with increasing transistor sizes, the resistance (R) goes down as the result of smaller pull-up resistors, keeping the RC product almost constant.

4.5 MCML sequential element versus CMOS

This subsection briefly compares the speed and SEU immunity of MCML with CMOS. A D flip-flop has been simulated in 90 nm technology, and the clock-to-Q delay has been measured to be 105 picoseconds, which is 1.6 times slower compared to a MCML flip-flop with a worst-case delay of 65 picoseconds. We used the same current source model to simulate a single-event strike as in the MCML case. The Q_{crit} for the CMOS flip-flop is 3.24 fC. For the MCML flip-flop at the same frequency (0.5 GHz), Q_{crit} values of 5.98 fC and 8.49 fC were achieved for a bias current of 500 µA at output voltage swings of 400 mV and 500 mV, respectively. However, the cost of power consumption and area at these MCML design points is very high. At lower bias currents, the Q_{crit} value is less for MCML than CMOS. For example, at a bias current of 100 µA, Q_{crit} is 2.83 fC for an output voltage swing of 500 mV, which is 1.14 times less than that of CMOS. The comparison was done at 0.5 GHz, at which both CMOS and MCML can operate accurately. However, at high frequencies, it is difficult to achieve functionality with CMOS, and it is therefore impractical.

4.6 Optimized design for SEU tolerant MCML

Based on the above results and analysis, for a clock frequency of 0.5 GHz, to design a MCML with a Q_{crit} value close to CMOS (3.2 fC), a bias current of 100 µA and output voltage swing of 400 mV are the optimized design parameters in terms of power consumption and area. This results in a Q_{crit} value of 2.7 fC. However, if an application can accommodate a bias current as high as 500 µA, the Q_{crit} value increases to 5.98 fC at the same output voltage swing.

At a clock frequency of 4 GHz, where CMOS becomes impractical for this technology, the same design choices (bias current of 100 µA and output voltage swing of 400 mV) result in a Q_{crit} value of 3.92 fC, which is 1.2 times better than CMOS at 0.5 GHz.

5. Conclusion

High-speed communication systems and mixed-signal environments exploit MCML in their circuits. Therefore it is important that MCML sensitivity to SEU be investigated and the effects of different design parameters on SEU be analyzed. The effects of several design parameters on critical charge have been thoroughly studied in this paper. Critical charge is the figure of merit in radiation effects, thus it is used as the indication of SEU hardening in this study. The effect of bias current, output voltage swing and operating frequency have been shown and discussed from the simulation results.

Based on these results, as the bias current increases, the critical charge increases as well. This is due to an increase in transistor sizes as bias current increases. The larger the transistors, the larger their capacitances are, which translates into larger critical charge. Simulation results show that critical charge can increase up to 5 times if the bias current changes from 30 µA to 100 µA.

This improvement in SEU immunity is at the cost of an increment in power consumption. Another parameter that has been swept for different values is output voltage swing. As output voltage swing increases, the critical charge increases as well due to an increased margin on effective voltage of the cross-coupled transistors in the hold stage. This results in a larger critical charge and consequently makes the node more SEU tolerant. Simulation results show that the critical charge is increased more than 2 times when voltage swing is increased from 300 mV to 500 mV at a bias current of 30 µA. Increasing the critical charge by amplifying the output voltage swing does not add to the power consumption, since the bias current stays unchanged. However, the area increases due to larger resistances in the pull-up circuit. Clock frequency has been altered from 0.5 GHz to 4 GHz in order to see the dependency of critical charge on speed. The results indicate that critical charge is independent of clock frequency until it reaches a frequency threshold. When this threshold is reached, critical charge increases with clock frequency. This threshold is hit when the clock period becomes smaller than the time a single-event strike needs to create free charge at the sensitive node. Results show that critical charge is almost 1.3 times more at 4 GHz than 1 GHz. Changing the above mentioned factors has a small effect on MCML delay since the RC value stays almost constant.

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