

SINGLE-EVENT EFFECTS CHARACTERIZATION AND SOFT ERROR MITIGATION IN 90nm COMMERCIAL-DENSITY SRAMs

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ABSTRACT

SRAM reliability faces serious challenges due to radiation-induced soft errors in aggressively scaled CMOS technologies. The increasing frequency of single-bit upsets and more recently multi-bit upsets (MBU) limits the efficacy of conventionally used single-bit error correcting codes (ECC). Additionally, techniques used in achieving dense packing of SRAM cells may potentially increase the single-event latchup sensitivity of these technologies. To characterize these single-event effects (SEE) for SRAMs in sub-100nm technologies, two prototype SRAM ICs have been designed in two characteristic 90nm bulk-CMOS commercial processes. To evaluate the effectiveness of soft error mitigation techniques, especially in the presence of MBU, two different ECC schemes with increasing error correction capability were implemented. SEE irradiation tests performed on these SRAMs reveal that MBUs are the dominating contributor to overall soft error rate, and their range could be as large as 13-bits. These test results validate the effectiveness of a mathematical model that shows how an effective bit error rate of 10^{-10} errors/bit-day can be achieved. Tests also show improved resilience of these technologies against single-event latchup, provided supply voltages are 1.1V or below.

KEY WORDS

VLSI circuits and systems, single-event effects (SEE), soft errors, radiation-hardening, SRAM

1. Introduction

With aggressive technology scaling, radiation-induced soft errors have become a major threat to SRAM reliability [1], especially for space electronics where galactic cosmic-rays (GCR) carry much higher linear energy transfer (LET) particles than terrestrial cosmic-rays and alpha particles from chip packaging, thus potentially inducing even larger multi-bit upsets (MBU) than previously reported [2][3]. SRAM cells are designed with minimum geometry devices (with special foundry design rule waivers from the standard logic design rules)

to increase density and performance, resulting in reduced critical charge (Q_{crit}) to upset cells [4].

The increased SRAM reliability issue, both due to single-event upset (SEU) [5] and single-event transient (SET) [6], has resulted in the development of radiation hardening approaches to reduce the SRAM bit error rate (BER) within acceptable reliability margins. In a circuit-based radiation hardening approach, both the individual memory cell and peripheral control circuits of a memory array are hardened with circuit and layout radiation-hardening-by-design (RHBD) techniques [7] and/or using specific processes at specialized hardening-by-process foundries [8]. The overall error rate of the SRAMs designed using these techniques is dominated by the raw bit error rate (raw BER) of the individual memory cell. The conventional radiation hardening processes face serious challenges due to their low-volume market and deficient performances as they lag by at least two technology generations compared to commercial counterparts. On the other hand, the associated area, power and speed penalties of RHBD circuit techniques are large and potentially offset the benefits of using state-of-the-art processes [9]. Alternatively, a more robust system-based hardening approach improves the effective error rate of the memory system over its raw BER by employing error correcting codes (ECC) and/or periodic memory scrubbing (a process in which memory contents are periodically checked for errors and written back after ECC correction to reduce the accumulation of errors). Therefore, usage of ECC such as single-error-correcting (SEC) and/or single-error-correcting-double-error-detecting (SEC-DED) codes is prevalent to protect memories from soft errors [1][10][11][12].

In the presented SRAM designs, we use a hybrid approach that hardens only the ECC encoder/decoder and control circuitry of a memory array using RHBD circuit and layout techniques, while leaving the commercial-density SRAM cell intact. The overall low effective BER is obtained through the combination of ECC, bit interleaving, and memory scrubbing [13]. This general approach has been advocated to be an effective approach to mitigate soft errors [1][10][14]. As embedded memories occupy increasingly large portions of system-on-chip designs (50% to 70%, or even more [4]), this

approach yields improved, denser hardened SRAM arrays than either a pure circuit-oriented or a system (ECC)-oriented approach alone, and will also continue to scale with technology improvements.

In this work, we present the design and single-event effect (SEE) irradiation test results of the two prototype SRAM ICs that have been designed in two characteristic 90nm commercial processes following the above mentioned approach to achieve a target effective BER. Particularly, a hybrid approach of mitigating soft errors is adopted where: 1) a foundry-distributed 6T SRAM cell is used as-is (no RHBD), 2) larger interleaving factors of 8 and 16-bits are implemented, 3) combination of periodic scrubbing and ECC are used in conjunction with a double-error-correcting (DEC) ECC in addition to the SEC-DED ECC, and 4) ECC encoder/decoder and other control circuitry is hardened using RHBD techniques. The application of two different ECC schemes is important from the standpoint of evaluating their relative efficiency in mitigating soft errors in a given radiation environment. In addition, it also provides two different data points for validation of our previously reported mathematical model [13]. The irradiation tests not only characterize the intrinsic radiation response of the two characteristics processes in commercial 90nm technology, but also help in investigating the true range of MBU in sub-100nm processes. This investigation provides insights for the selection of ECC architectures in future technologies. In addition, the single-event latchup (SEL) test results reveal interesting characteristics for latchup sensitivity/resilience of these commercial-density SRAMs.

The rest of the paper is organized as follows. In section 2, we briefly describe the design highlights of the prototype SRAM ICs including the parallel decoder design for double error correcting BCH (Bose-Chaudhuri-Hocquenghem) codes. Section 3 presents our SEE test results, both for single-event upset and single-event latchup tests, showing the true range of MBU and SEL sensitivity/resilience in these processes. In section 4, we present test results, validating a mathematical model for mitigating soft errors and showing relative efficiency of the two ECC schemes. Section 5 concludes the paper.

2. Design Description

Two prototype SRAM ICs are developed in two characteristic processes of commercial 90nm bulk-CMOS technology. One chip is designed in a low-power process, and henceforth we label it as LP; the other chip is designed in a standard fabrication process labelled SF. The core supply voltage is 1.2V for LP SRAM and 1.0V for the SF IC, while the I/O supply is 2.5V for both ICs. Each test chip further contains two memory modules, one labelled *baseline* module and the other labelled *hardened* module. The baseline module does not apply any of the radiation hardening techniques, neither on the memory array nor on the peripheral logic. This serves as a basis to

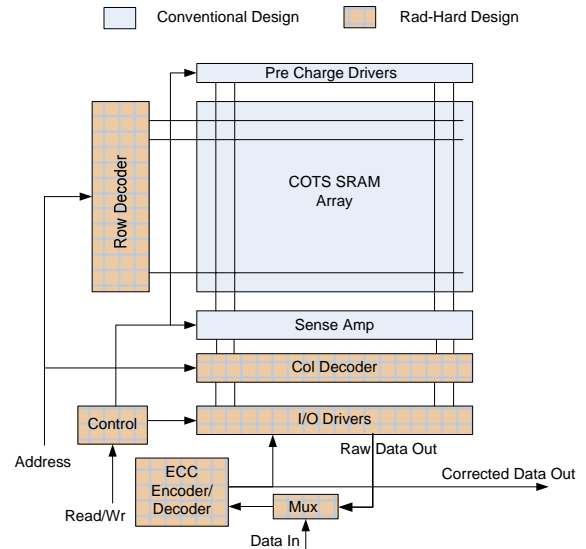


Figure 1. Block diagram of SRAM hardened module

characterize the process's inherent response to irradiation. Each hardened module, on the other hand, uses the proposed hybrid approach with ECC hardening for the memory array and TMR (triple modular redundancy) for hardening the peripheral logic against single-event transients including the ECC encoder and decoder circuits. Figure 1 depicts the block diagram of a hardened SRAM module, showing the core memory array using a commercial design while highlighting blocks that are protected by RHBD techniques. Note that RHBD techniques have not been applied to pre-charge drivers and sense amplifiers due to the pitch-matching layout constraints with the core array. Increasingly large interleaving factors are implemented to separate physically adjacent bits into disjoint logical words such that the LP hardened SRAM uses an interleaving factor of 8 while the SF SRAM employs interleaving by 16.

For analyzing the relative reliability efficiency of ECC techniques, the two implemented ECC techniques include a Hsiao SEC-DED (21, 16) code [15] in the LP IC and a double error correcting BCH (15, 7) code [16] in the SF IC. The size of the baseline array is 64-kbits in each IC while the size of the hardened array increases in accordance with the extra bits required for a particular ECC applied in each case. Therefore, the LP hardened SRAM module contains 90112-bits while the SF hardened module contains a total of 122880-bits. Notice that the ECC overhead decreases as the block size increases and therefore if a DEC code is applied on a larger word size, the overhead of check bits would be reduced significantly [16]. The Hsiao SEC-DED decoder is designed following the architecture described in [15]. To suit the memory application's word-wide accesses, the BCH decoder is designed to operate on a whole word in parallel as opposed to the traditional Berlekamp-Massey, Euclidian or minimum-weight sequential decoding schemes [16][17][18]. In the following, we briefly describe this decoder architecture.

2.1 Parallel DEC BCH Decoder

The parallel decoding technique for double error correcting BCH codes is based on the standard array decoding procedure [16]. A block diagram for this standard-array based decoder is shown in Figure 2, and it consists of three main parts: 1) Syndrome Generator, 2) Error Pattern Decoder and 3) Error Corrector. The circuit for the syndrome generator is similar to a conventional XOR tree-based encoder circuit which computes the check bits using data inputs specified in the code and compares with the received check bits. In case of no error, a zero syndrome is generated. Alternatively, a non-zero syndrome is generated if the computed check bits are not matched to the received check bits. Therefore, a bit-wise ‘OR’ of the syndrome bits is used to flag an error occurrence. An error pattern decoder circuit is implemented using combinational logic that maps each correctable error pattern to a unique syndrome. Associated pairs of correctable error patterns (\underline{e}) and syndromes (\underline{s}), required for this mapping, are pre-computed by multiplying correctable error patterns with the parity check matrix H of the code. For binary vectors, an erroneous bit is corrected merely by complementing it; therefore, the error corrector circuit is simply a stack of XOR gates.

3. SEE Test Results

Both SRAM ICs have been extensively tested for single-event effects (SEE). The SEE tests were performed at the Lawrence Berkeley National Laboratories (LBNL) 88-inch cyclotron in accordance with the EIA/JEDEC standard. The heavy-ion-induced single-event upset characterization used a 10 MeV cocktail beam, as it has optimal ion energies, LETs and ranges (penetration depth) for this experiment. Table I shows the ions, their energies and LETs in the 10 MeV cocktail beam. Note that the 2 highest ‘effective’ LETs were obtained by performing tests in an angled strike condition. All tests were run to a total fluence of 1×10^7 particles/cm², until at least 200 errors were recorded or until a destructive or functional perturbation in the device under test occurred. The primary goal of the SEU testing was to determine the

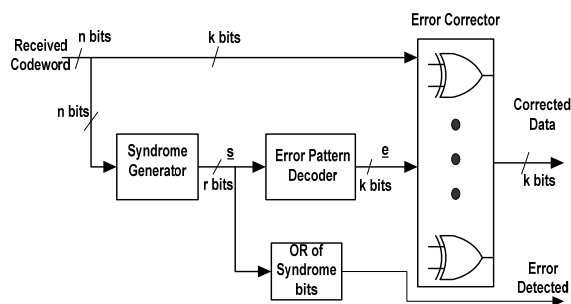


Figure 2. Block Diagram of BCH Decoder

TABLE I. 10 MEV COCKTAIL IONS USED DURING THE SEE TESTS

Ion	Energy (MeV)	LET (MeV-cm ² /mg)
B	108	0.89
O	184	2.19
Ne	216	3.49
Ar	400	9.74
Mn	541	16.88
Cu	659	21.03
Kr	886	30.85
Xe (normal)	1330	59.08
Xe (30° strike)	1330	67.8
Xe (60° strike)	1330	117.44

parameters relevant to BER calculations, i.e., the threshold LET and the sensitive cross-section of each SRAM device. The SRAMs were tested in vacuum for the -10% nominal voltage worst condition for each IC.

3.1 SEU Cross-Section

For test completeness, the SRAMs were exposed under a variety of loaded bit patterns (consisting of all 1, all 0 and checkerboard patterns), to investigate any possible pattern-sensitive dependence. Additionally, tests were conducted on the SRAMs for both *static* and *dynamic* operating modes. In static mode, the memory content was not accessed during irradiation, leaving the peripheral/control circuitry of the core SRAM array inactive. In the dynamic mode, the memory content was continuously read/written back during irradiation, therefore continuously activating the same peripheral/control circuitry previously left inactive in the static test. Any noticeable cross-section difference between the two operating modes would indicate a sensitivity of the peripheral/control circuitry to single-event transients, as this circuitry mostly consists of combinational logic elements.

Figure 3 (a and b) presents the raw SEU cross-sections of the LP baseline and hardened SRAMs respectively, showing the true radiation response of each SRAM module: before any error correction (if applicable) is performed. Similar tests were performed for SF baseline and hardened SRAMs. For compactness and comparative analysis, Figure 4 shows the resulting upset cross-sections for both ICs, based on uncorrected data for baseline and hardened modules. Each curve is a Weibull best fit to data points calculating the ratio between errors counted at the uncorrected output of the SRAM to the total number of particles to which it was exposed, normalized to the total bits in each module. All SEU cross-sections (LP and SF, baseline and hardened) showed a very low onset LET. Upsets were always observed for the lightest ion available in the 10 MeV beam cocktail. Using the common definition of ‘threshold LET’ (LET at 10% of saturating cross-section), we

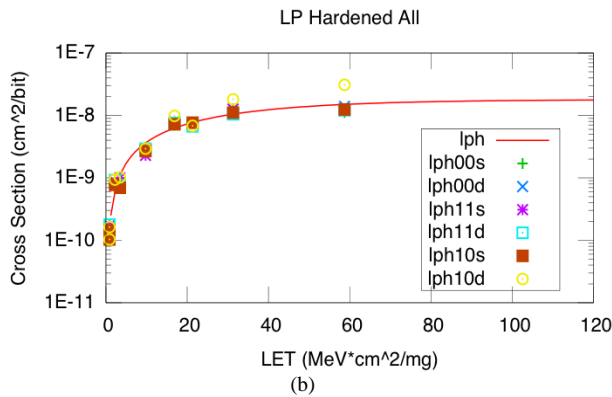
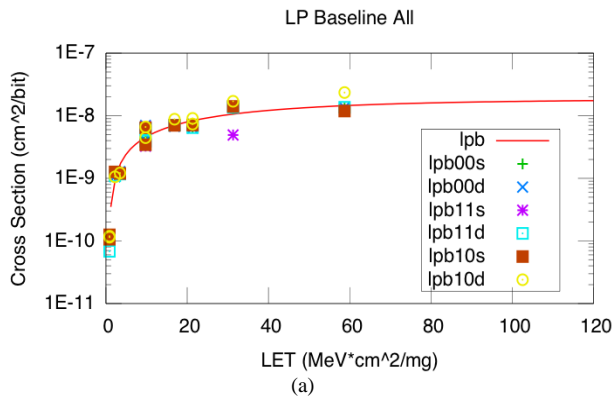


Figure 3. SEU raw cross-section for the LP Baseline (lpb) and Hardened (lph) SRAMs. Each data set specifies the data pattern loaded and the operating mode: static (s) or dynamic (d)

determined that LET_{th} for these test ICs is $\sim 3\text{-}5 \text{ MeV}\cdot\text{cm}^2/\text{mg}$. The analysis of the LP and SF cross-section data did not show any clear pattern dependence of the SRAM's cross-section, as data points from the various loaded patterns overlapped across the range of tested ions and LET. Similarly, no sensible differences between static and dynamic testing conditions were observed, indicating that the peripheral circuitry has a very low error cross-section. In other words, the total error cross-section of each SRAM is dominated by the cross-section of its memory core. Note that the SF cross-sections are higher than the LP cross-sections across the range of tested LETs (twice as sensitive as LP at saturation). Such a difference

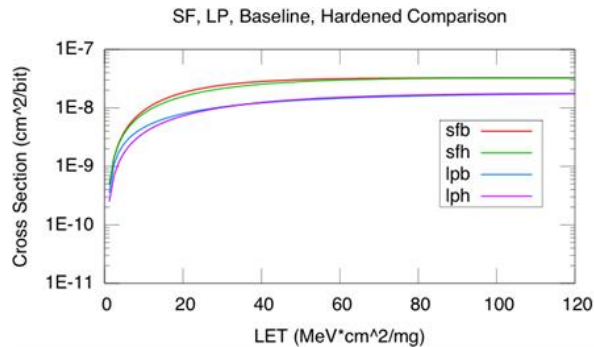
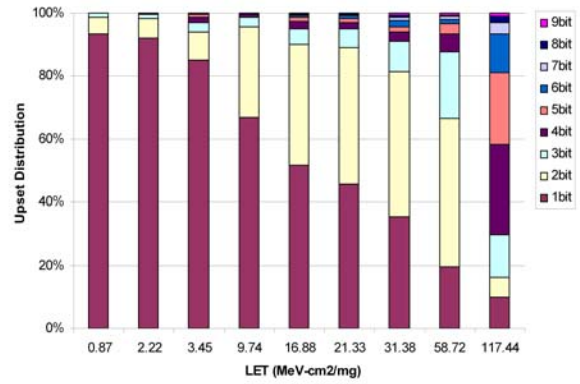
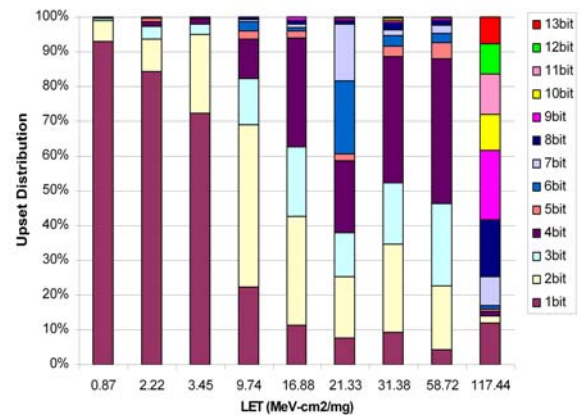


Figure 4. Best fit Weibull curves for cross-section data for both LP and SF SRAMs



(a)



(b)

Figure 5. Single and Multi Bit Upset Distributions versus Effective LET (a) LP SRAM (b) SF SRAM

in sensitivities may be related to the lower operational Vdd of the SF technology affecting the critical charge for each SRAM cell.

3.2 SBU/MBU Distribution

Figure 5 shows the distribution of upsets for LP and SF SRAMs versus ion LET value. At onset, single-bit upsets (SBU) dominate the total soft error distribution; however MBU quickly become the main contributor as the LET increases. A wide difference in MBU distribution can be noted for the two ICs, in addition to observing that the largest MBU is 9 bits for LP versus 13 bits for SF. The difference in distribution can be understood by investigating the critical charge of the 6T SRAM cell in each process. Our simulations show that the Q_{crit} of the LP cell is slightly higher than the SF (1.58fC vs. 1.23fC), due to variations in cell design and nominal operating voltages (1.2V and 1V , respectively). These MBU distributions potentially suggest that much larger interleaving factors should be implemented in order for the errors to appear random and be effectively handled by an ECC model. If an increasing MBU trend continues with technology scaling, it would become necessary to adapt to more powerful codes such as DEC ECC.

3.3 Single-Event Latchup Sensitivity

To completely characterize the SEE response of the devices, latchup experiments were also conducted on the LP and SF SRAMs. Since commercial SRAM core memory violates standard logic design rules to achieve commercial density, it makes it even more susceptible to latchup. Particularly, the decreased spacing between wells and diffusions of interest, in addition to the elimination of P+ taps (substrate grounds), have the potential to be very harmful to the latchup resilience of the SRAMs.

Considering the worst case scenario, the devices were tested at +10% V_{dd} and at a temperature of 125°C. The SF SRAM exhibited total resilience to latchup for all tests upto an effective LET of 118 MeV-cm²/mg, for a total fluence of 2x10⁷ particles/cm², without any effect on the SRAM operation (baseline and hardened). Under worst-case test conditions, the LP SRAMs exhibited a very high sensitivity to latchup. Latchup was triggered in the LP SRAMs almost instantaneously, for LETs as low as 2.18 MeV-cm²/mg. The identification of such a low latchup threshold prompted additional tests, revealing some interesting observations. Firstly, the trigger and release voltages for the latchup phenomenon were identified around 1.10 - 1.14 V. This means that if V_{dd} was kept at 1.1V or below, no latchup was triggered up to an LET of 118 MeV-cm²/mg at 125°C. Secondly, temperature was also shown to play a crucial role in triggering latchup. We tested the SRAM up to the maximum LET (118 MeV-cm²/mg) at +10% V_{dd}, but at room temperature (25°C), without registering a single latchup event. Finally, none of the SEL was destructive: all the parts worked perfectly after power-cycling to remove the latchup state. These results indicate that in current and future technologies where supply voltages are 1.1V or below, the processes are intrinsically immune to single-event latchup. This represents a positive outcome of technology scaling towards single-event effects and potentially enhances the interest of using commercial-of-the-shelf (COTS) electronics for space applications.

4. Model Validation

In order to validate our previously reported theoretical model of mitigating soft errors [13], we compare the model's effective BER predictions to experimental data measurements. As per the model, the effective BER of a memory protected by a single error correcting ECC can be approximated by (1):

$$EffectiveBER_{(SEC-ECC)} \cong \frac{rawBER}{1 + \left[\frac{ScrubRate / rawBER}{300} \right]} \quad (1)$$

Similarly, equation (2) approximates the effective BER of a memory protected by a double error correcting ECC.

$$EffectiveBER_{(DEC-ECC)} \cong \frac{rawBER}{1 + \left[\frac{ScrubRate / rawBER}{15} \right]^2} \quad (2)$$

TABLE II. ECC MODEL PREDICTIONS VS. SEU EXPERIMENTAL DATA

	LPH Static	SFH Static	LPH Dynamic	SFH Dynamic
Scrub Rate /bit	1 / Run		2.22 kHz	0.718 kHz
Raw BER	Errors / Run / Memory Size		Errors / Run / Time (Sec) / Memory Size	
Effective BER	Eq. 1	Eq. 2	Eq. 1	Eq. 2
Total SBU (All SEU Runs)	13,004	12,117	9,901	9,372
Errors Observed	7,305	195	NO ERRORS	NO ERRORS
Errors predicted	7,633	187	6.7 (< 1 word)	0.0002

The prediction capability of this model is corroborated in Table II, where we compare in the last two rows 1) the total number of errors still observed after ECC correction attempt, with 2) the total errors predicted by the model that would not be corrected, for the given raw BER of the SRAM cell, scrub rate and ECC.

For the static test condition, experimental data shows that for the LP hardened SRAM, the single error correcting ECC reduced the error count by ~44%. In the SF hardened SRAM case, using a double bit correcting ECC, the error count was reduced by ~98.5%. These results indicate the relative reliability performance of single and double error correcting ECC schemes whereby we observe that a double error correcting ECC reduces the error count more than twice that of a single error correcting ECC. It is to be noticed that though double error correcting ECC performs significantly better than single error correcting ECC, without scrubbing it also cannot mitigate all induced errors. Alternatively, for the dynamic test condition where the memory was periodically scrubbed, the LP and SF hardened SRAMs did not register a single uncorrected error during the experiment. The ECC schemes were always able to output a correct codeword, regardless of the faulty bits in the memory array. Notice that relatively higher scrubbing rates were used due to a constant high flux of ionizing particles during the accelerated tests for both ECC schemes. These results demonstrate that the theoretical model's prediction capability is excellent, where the model overestimates by only ~4.5% the number of uncorrected errors in the static operating mode. The agreement with the dynamic test results is even better; the difference is less than 0.1%. Therefore we can conclude that the model can be confidently used to assess the resilience of such SRAMs in various space environments and benchmark performance to an application's soft error reliability requirements.

5. Conclusion

Two 90nm SRAM IC designs developed by following a hybrid radiation hardening approach for mitigating soft errors have been presented. The heavy-ion irradiation test

results reveal that for large LETs, multi-bit upsets (MBU) are the dominating contributor toward overall soft error rate. Furthermore, it is observed that heavy-ions from galactic cosmic rays can induce very large MBU clusters: up to 9 bits for LP technology and up to 13 bits for SF technology. This suggests that traditional ECC approaches cannot completely mitigate resulting soft errors and some of the following techniques must be used: 1) very large interleaving factors, 2) stronger codes such as DEC ECC, 3) periodic memory scrubbing, or 4) a combination of these approaches. The presented data also validates a mathematical model that relates ECC strength and scrubbing in mitigating soft errors, which makes it possible to estimate scrubbing rates in order to meet a target reliability with any given ECC. Additionally, the intrinsic single-event latchup immunity of commercial processes in scaled technologies (for supply voltages 1.1V or less) makes commercial-off-the-shelf (COTS) technologies much more attractive for space applications, provided suitable RHBD techniques are applied to obtain desired effective error rates.

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