

A High-Speed Fully Differential Current Switch

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Abstract

A high-speed fully differential current switch is presented. The clock-feedthrough effect is reduced by Swing-Reduced Drivers and neutralized by dummy transistors. With the use of Swing-Reduced Drivers (SRD), less charges are required to be transferred to/from the gates of the switching transistors, and hence, the switching speed can be increased without significant output error. The SRDs also reduce the possible large current spikes on the outputs of the current switch. Analysis shows this current switch is ideal for high-speed current-mode $\Sigma\Delta$ processing. A continuous-time switched-current $\Sigma\Delta$ modulator using these current switches has been implemented in a $2\mu\text{m}$ CMOS process and achieved a 50 dB dynamic range with a 50 MHz clock.

1. Introduction

The CMOS switched-current (SI) technique has been widely used for sampled-data analog processing in recent years. SI circuits use MOS transistors as the storage elements to provide an analog memory capability. Recent research shows, however, SI circuits can also be used for high speed semi-continuous-time signal processing, such as continuous-time switched-current $\Sigma\Delta$ modulators [1], as shown in Figure 1. This use requires SI circuits to operate at even higher speeds.

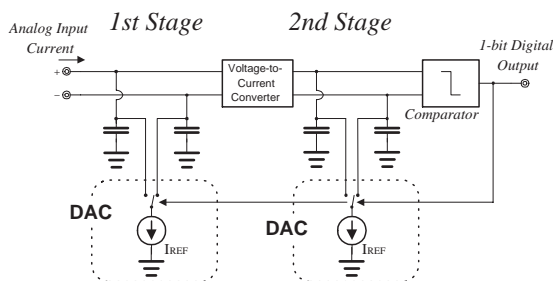


Fig.1: A second-order continuous-time switched-current $\Sigma\Delta$ modulator.

However, serious problems in SI circuits are switch-induced errors, or the *clock-feedthrough* (CFT) effect. Without efficient clock-feedthrough cancellation, it is impossible to realize high-speed switched-current circuits with acceptable accuracy. A number of solutions have been proposed [2] – [8].

A technique commonly used for cancellation of the clock-feedthrough effect is to add a half-sized “dummy” MOSFET as shown in Figure 2. This technique requires two clock phases, and its accuracy is critically dependent on the timing relationship between the clock phase edges, which is very difficult to control.

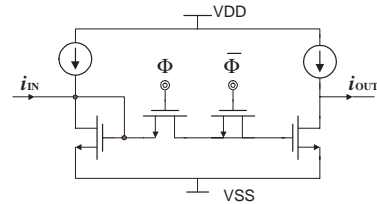


Fig.2: Charge cancellation in a SI circuit using a dummy MOSFET switch.

Some other techniques use replication (Fig. 3) [2] or multi-path cancellation [3] – [5] which requires a cancellation current ripple through current mirror(s). The delay of the current mirrors limits the operation speed of the current switches.

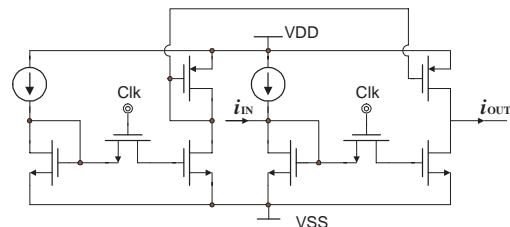


Fig.3: Charge cancellation using replication.

SI systems based on a fully differential architecture have been presented in several papers recently [6][7]. The delay of the current mirrors is no longer a problem in

this kind of circuit. However, large common-mode output current spikes may be induced by a steep clock edge. A slower clock with slow rise and fall times is required for this kind of application. Another solution is to use some charge attenuation technique [8]. However, the speed is limited by the additional capacitors and the use of multi-clock phases.

In this paper, a fully differential current switch circuit is proposed. The clock-feedthrough effect is neutralized by dummy transistors without rippling through current mirrors. The common-mode current spikes are attenuated by Swing-Reduced Drivers.

2. Circuit Design

The proposed high-speed current switch is composed by an NMOS differential pair as shown in Figure 4. The possible common-mode output current spike is reduced by reducing the voltage swing on the gates of the switching transistors (M1 and M2). The Swing-Reduced Drivers (SRD) are used to reduce the voltage swing on the gates of the switching transistors. By reducing the voltage swing, the charges which are transferred to/from the gates are also reduced. This greatly reduces the transistors' switching transition times. The D-type flip-flops (DFF) are used to synchronize the switching. Transistors M3 and M4 are two dummy transistors with the same sizes as M1 and M2 to neutralize (cancel out) the feed-through charges.

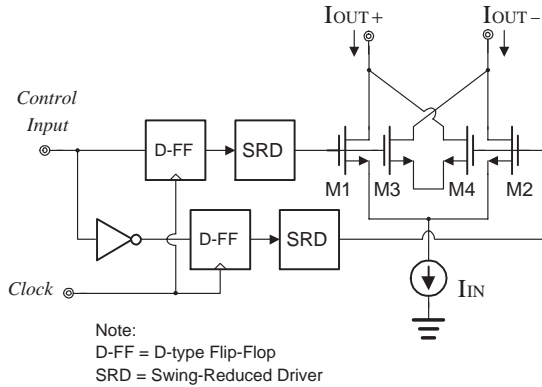


Fig.4: Proposed high-speed current switch

For systems which require the current switch to **return to zero**, the current switch can be implemented as depicted in Figure 5. M5 and M6 are used to stabilize the common-mode output current during the return-to-zero state. For some systems, the common-mode output current must be stable (not changing rapidly) to maintain the stability of the common-mode voltage, and therefore, M5 and M6 are required for the stability of these systems.

However, a mismatch between M5 and M6 will cause an output offset current. M5 and M6 also reduce the output impedance of the current switch during the return-to-zero state. This may affect the pole and zero locations of the system. For continuous-time switched-current $\Sigma\Delta$ modulators, a reduction of output impedance reduces the low-frequency open-loop gain of the integrator, and leads to more in-band noise.

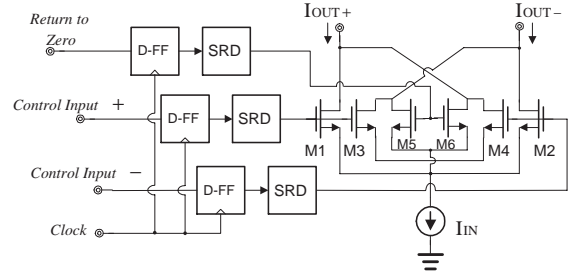


Fig.5: Proposed high-speed current switch with "return-to-zero" state

Figure 6 shows the circuit diagram of the Swing-Reduced Driver (SRD). M1 through M4 compose two inverters to drive M6 and M7. M5, M6, and M7 form a class-AB output stage. M8 and M9 serve as resistors to load the the output and maintain the voltage swing in the desired range.

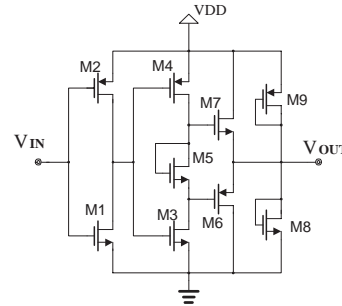


Fig.6: Circuit diagram of the Swing-Reduced Driver (SRD).

The output voltage swing range is determined by the threshold voltages and the sizes of M6 – M9. If the aspect ratio (W/L) of M6 – M9 are A_6 – A_9 respectively, the output high and low voltages of SRD, V_{OH} and V_{OL} , are

$$V_{OH} = \frac{\sqrt{A_7} V_{DD} - \sqrt{A_7} V_{THNB} + \sqrt{A_8} V_{THN}}{\sqrt{A_7} + \sqrt{A_8}}$$

$$V_{OL} = \frac{\sqrt{A_9} V_{DD} + \sqrt{A_9} V_{THN} - \sqrt{A_6} V_{THNB}}{\sqrt{A_6} + \sqrt{A_9}}$$

where V_{THNB} and V_{THPB} are the threshold voltages of the NMOS and PMOS transistors, respectively, with body effect. By manipulating A_6 – A_9 , a desired voltage swing range can be achieved.

3. Performance of the Current Switch

3.1. Output Voltage Range

Clock-feedthrough cancellation is achieved by the dummy transistors M3 and M4 in figure 4. M3 and M4 are geometrically the same as M1 and M2 for the ease of matching capacitance. The sources of M3 and M4 are floating and follow the gate voltages of M3 and M4, and hence, they are always **off**, with no channel formed. The only capacitances are the gate-to-drain overlap capacitors. To ensure cancellation, M1 and M2 must be in either the saturation region or the cut-off region.

If the voltage of either of the output nodes is lower than $V_{OH} - V_{THNB}$, the gate-to-drain capacitance (C_{gd}) of M1 or M2 is not simply just the overlap capacitance. Part of the gate-to-substrate capacitance will contribute to the gate-to-drain capacitance, and cause the cancellation to fail. Accordingly, the output voltages should stay above $V_{OH} - V_{THNB}$.

3.2. Maximum Switching Speed

The switching speed of the proposed current switch is no longer limited by the clock-feedthrough effect. In fact, even with $\pm 10\%$ mismatch of the sizes of M3 and M4, the induced error is less than 0.1%. The switching speed is limited, however, by the mismatch of the switch-on and switch-off speed. **The turn-off speed is faster than the turn-on speed for NMOS transistors.** This effect causes a delay when a NMOS transistor is turning on and a overshoot of the output current right after it turns on. The charges which are lost by the delay of the turn-on time are restored to the output. The net charges which are delivered to the output port are equal to the input current times the clock cycle, $I_{IN} \times T_{CLK}$.

Figure 7 shows the output current waveform of a current switch operating at 50MHz. The current switch was implemented in a $2\mu\text{m}$ CMOS process with the sizes of M1 to M4 equal to $8\mu\text{m} / 2\mu\text{m}$.

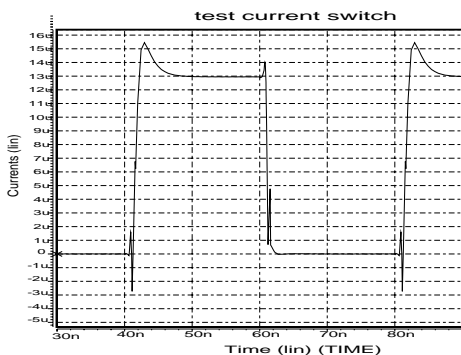


Fig.7: Output current waveform of a current switch operating at 50MHz

Analysis shows if the clock cycle is longer than the time interval of the overshoot output current, the error of the net output charges during one clock is very small. Figure 8 shows the net output charge error versus the switching frequency.

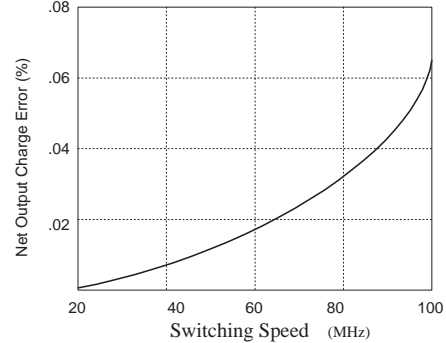


Fig.8: Net output charge error vs. Switching frequency.

3.3. Clock Skew Effect

Another effect which can cause error on the output is skew between the two control nodes (gates of M1 and M2). The D-type flip-flops (DFF) are used to minimize this effect. However, the skew may be caused by a speed mismatch of the PMOS and NMOS transistors in DFFs and SRDs. If the skew is too large, M1 and M2 may turn on at the same time and M1 – M4 then compose a differential amplifier with positive feedback. This may cause the current switch circuit to oscillate. Figure 9 shows the relationship between the net output charge error and the skew.

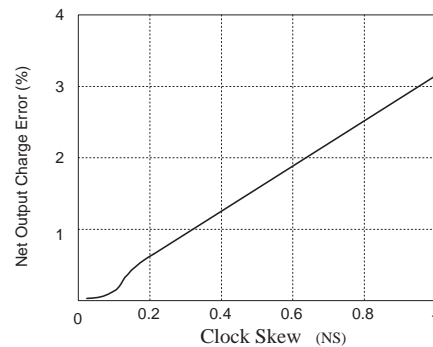


Fig.9: Net output charge error vs. clock skew.

4. Experiment result

The proposed current switch has been implemented in a continuous-time switched-current $\Sigma\Delta$ modulator in a $2\mu\text{m}$ CMOS double-poly double-metal process as shown in Figure 10. The current switches function as 1-bit DACs

in the feedback loop of the modulator as shown in Figure 1. From analysis and simulations, the current switch has less than 0.1% error with a switching speed up to 100MHz.

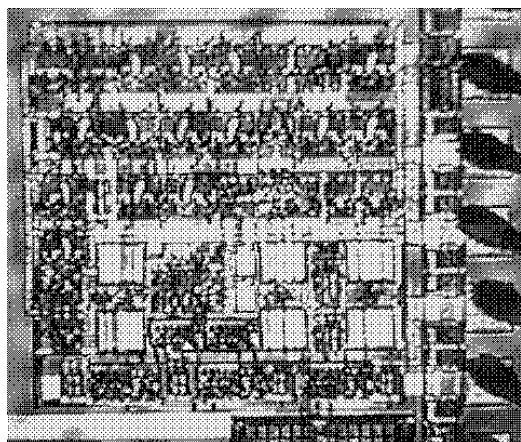


Fig.10: Microphotograph of the $\Sigma\Delta$ modulator.

The measured result shows the complete modulator has a 60 dB dynamic range with a clock up to 60MHz. The clock speed is limited by the comparator, not the current switches.

Table 1: The experimental result

The Current Switch	
$V_{POWERSUPPLY}$	5V
Operation Speed	$\leq 100\text{MHz}$
V_{OH} of SRD	2.5V
V_{OL} of SRD	1.75V
Minimum V_{OUT}	1.8V
Clock induced error	$< 0.1\%$
$\Sigma\Delta$ modulator	
$V_{POWERSUPPLY}$	5V
Clock frequency	20MHz \sim 60MHz
Signal Bandwidth	1MHz
Dynamic range	60 dB
Reference current	10 μA
Input current range	$\pm 5\mu\text{A}$
Power dissipation	16.6 mW @50MHz
Active area	0.37 mm^2 (620 \times 600 μm)
Technology	2 μm CMOS

5. Conclusion

A new high-speed fully differential current switch is presented. The clock-feedthrough problem has been successfully solved. With the help of the Swing-Reduced Driver

(SRD), the current switch can operate up to 100 MHz with less than 0.1% error when implemented in a 2 μm process. A continuous-time switched-current $\Sigma\Delta$ modulator using this current switch has been implemented, demonstrating the superior performance of this current switch.

Acknowledgements

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