

DF-DICE: A Scalable Solution for Soft Error Tolerant Circuit Design

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Abstract—The Delay Filtered Dual Interlocked storage Cell (DF-DICE) offers a scalable solution in different radiation environments for soft error mitigation. The area and speed performance for five different single event transient thresholds have been evaluated. The results show that the cost of soft error mitigation is minimal for terrestrial environments (overall area penalty less than 14% and speed penalty within 6% for flip-flop based typical designs) while it is larger for space environments (overall area penalty up to 30% and speed penalty up to 13% for flip-flop based typical designs). The logic of a conventional Application Specific Integrated Circuit (ASIC) can easily be converted to a soft-error tolerant design by replacing the existing storage elements with the respective DF-DICE elements.

I. INTRODUCTION

Soft errors pose a major threat to system reliability in today's deep sub-micron technologies. Technology scaling relies on reduced node capacitances and lower voltages to improve performance and smaller dimensions to increase density. On the other hand these small values of node capacitances and reduced nominal voltages lower the critical charge (Q_{crit}) required to upset a node and make these technologies more susceptible to soft errors. The increased densities of modern chips make it more probable to have a large number of soft errors. It is predicted that the Soft Error Rate (SER) per chip of logic circuits will increase exponentially till 2011 [1]. Due to the increasing severity of the soft error problem, there is a growing trend in the community to adopt soft error rate as a design parameter along with power, area and speed trade-offs [2].

Single Event Upsets (SEU) in memory elements have been long recognized as a reliability problem. It is now customary to protect memories with Error Correcting Codes (ECC). There are various solutions presented in literature to protect random sequential logic (latches and flip-flops), for example Triple Modular Redundancy (TMR), Heavy Ion Tolerant (HIT) cell [3], Single Event Resistant Topology (SERT) [4], and Dual Interlocked storage Cell (DICE) [5]. Transients generated in combinational logic were not

considered important because of the inherent immunity of combinational circuits due to logical, electrical and latching window masking of these transients [6]. Only recently, due to lower transition voltages and higher frequencies in deep sub-micron technologies, Single Event Transients (SET) generated in combinational logic by incident ionizing particles are becoming increasingly pronounced. These transients not only occur in combinational logic, but may happen in clock lines and global control signals. They may result in SEU if propagated to the data input of a storage element within the window of vulnerability of that element. Alternatively they may result in an erroneous clearing or setting of the state of the storage element if they appear on global control lines. The temporal sampling latch [7] provides a solution for SET mitigation as well as SEU mitigation. However, it does not mitigate transients on the asynchronous control signals. In [8] we have presented a solution that combines the principle of delay filtering and DICE cells to mitigate SETs up to 800ps as well as SEU.

In this paper we extend our work described in [8] to scale it to various radiation environments. The described cells provide soft error mitigation for SEU as well as SET on any of the inputs of the storage elements, thereby taking care of the transients generated in the combinational logic. In this paper, we show that the cost of filtering an SET is linearly related to the width of the transient pulse. Since there is a linear relationship between the width of the transient pulse and the Linear Energy Transfer (LET) of the incident ion [9], we show that the cost of soft error mitigation is proportional to the desired SET tolerance. Also, by characterizing the environment of operation with the LET spectra of incident particles, we demonstrate that SET mitigation is a strong function of the radiation environment. For instance, for terrestrial environments where the LET of ionizing particles is low, the increase in area and reduction in operating frequency is minimal. While in space, where ions have higher LET values, the area cost and the reduction in speed is larger.

The rest of the paper is organized as follows. Section 2 summarizes radiation environments and previous work. In

Section 3 we describe scalability scenarios for DF-DICE in different radiation environments. Section 4 discusses implementation and results, and in Section 5 we conclude the paper.

II. BACKGROUND

A. Radiation Environment

In terrestrial environments, high-energy neutrons generated from the interaction of cosmic rays with the atmosphere are the main source of incident radiation. Neutrons cannot cause direct ionization, but the by-products of nuclear reactions with the silicon and Si-recoil reactions generate ionizing particles that cause soft errors. Alpha particles either generated from flip-chip packaging or from the decay of naturally occurring radioactive impurities in silicon are another cause of soft errors. The flux of neutrons is a strong function of altitude and respective data can be found in [10]. The interaction of thermal neutrons with ^{10}B (used as an insulating glass in many CMOS processes) leads to alpha particle generation and ^7Li recoil ions, which in turn deposit significant charge to cause single event effects.

The hostile environment in space is mainly composed of high energy protons and other heavy ions ranging from alpha particles to uranium. Trapped radiation in the earth's magnetic field (Van Allen belts) contains high energy protons and electrons. Solar flares also bombard high energy protons and heavy ions. These ions cause direct ionization of the struck material. The amount of charge generated in the device by the incident ion is characterized by Linear Energy Transfer (LET). Therefore Single Event Effects (SEE) are described with respect to LET instead of ion types. The LET spectra for space radiation can be found using environment modeling tools like CREME (Cosmic Ray Effects on Micro Electronics) [11]. It turns out that heavy ions in space have much larger LET values than the particles in terrestrial environments; therefore the effects in space are much more severe.

B. Previous Work

Traditionally space electronics, where radiation hardening is essential for reliable operation, were manufactured at designated foundries employing specialized processes to improve the radiation tolerance of electronic devices. This method of attaining system reliability has been known as Radiation Hardening by Process. With the changing economy of the space electronics market, these processes have begun losing ground due to their very high cost and poor performance (they usually lag the commercial processes by two generations). This has led to the development of Radiation Hardening by Design (RHBD) in which architecture, circuit, and layout techniques are used to mitigate radiation effects using commodity fabrication foundries.

Soft error mitigation techniques involve either spatial or temporal redundancy. The simplest spatial redundancy method, triple modular redundancy (TMR), replicates critical

circuit nodes (latches and flip-flops) three times and then a majority vote is used to ignore any corrupt value. This method suffers from large area and power penalties, but the speed degradation is minimal. Only the voter circuit affects the critical path for speed. The second class of spatial redundancy mitigation techniques replicates critical nodes (latches and flip-flops) and uses feedback to recover the correct value after an upset. The most commonly used SEU immune cells based on the above technique include the Heavy Ion Tolerant (HIT) cell [3], the Single Event Resistant Topology (SERT) [4], and the Dual Interlocked storage Cell (DICE) [5]. The HIT cell suffers from the drawback that the transistor sizes are critical in restoring the correct value after a single event upset. While the relative transistor sizes are important for DICE and SERT cells, attaining precise values is not necessary. Both DICE and SERT offer a comparable area solution, yet the DICE cell has been widely used in industry, and sufficient data is available in the literature about the SEU immunity of the DICE cell [12].

Temporal redundancy techniques are characterized by sampling the input data at time intervals spaced greater than the width of the transients to be tolerated and then voting the corrupt value out. The temporal latch [7] solution is based on this principal. The basic scheme uses three clocks to sample data at different time intervals and a fourth clock to synchronously latch the sampled data. It employs TMR to store temporally sampled values in three different latches and then uses a synchronous majority vote to forward the correct value. This design offers mitigation not only to SEU but also to SET on data input. Although a modified version of this latch can mitigate SET on clock inputs, this technique fails in case of transients on asynchronous control signals like clear and preset. Tripling the hardware and including the voter circuit significantly increases the area and power overheads. Furthermore, this design suffers from a large speed penalty which is at least equal to twice the targeted SET pulse width.

Techniques for filtering transients on data inputs have been presented in [13] and [14]. Since the approach in [14] requires dual-rail logic and is limited by relative transistor sizing, we focus on the approach of [13]. The basic principle is the same as temporal filtering. The optimized circuit in [13] achieves the filtering action using a C-element as shown in Fig. 1. The C-element is a state holding element, and it has

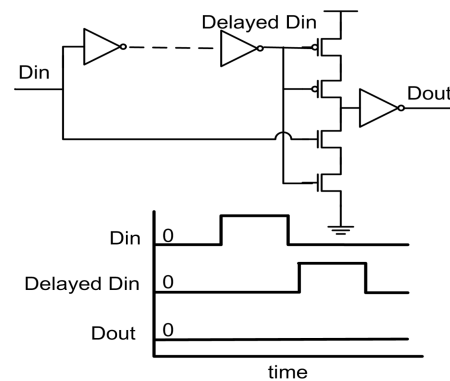


Figure 1. Delay Filter (DF)

the basic property that it changes its output only when all the inputs are of identical logic value. The incoming data signal is fed to the C-element using two paths: one with zero delay and the other with a delay of $T_{critical}$ (equal to the SET pulse width to be suppressed). Hence a transient of $T_{critical}$ width will not be able to change the output of the C-element.

III. SCALABILITY OF DELAY FILTERED DICE

The basic principle of the Delay Filtered DICE (DF-DICE) is to use delay filtering to filter out the transients on the input signals of the storage elements. The DICE storage cells mitigate the SEU occurring inside the element by spatial redundancy and active feedback. While transients can be tolerated only on data input in [14]; the structure of DF-DICE employs delay filters on all of its inputs to suppress transients generated either in combinational logic or on global control lines. A circuit for DF-DICE latch with preset and clear control signals is shown in Fig 2. The operation of DF-DICE is explained in detail in our previous work [8]. An important feature of the DF-DICE cell is that it can be scaled to mitigate transients of various pulse widths by changing the number of inverters in the delay chain. A direct on-chip measurement of SET pulse widths shows a linear relationship between the LET of incident ions and the pulse width of the generated SETs [9]. As the width of transients generated is different in different environments, a particular delay filter can be used to mitigate all the transients generated in a specific environment.

In terrestrial environments the main sources of radiation are alpha particles and by-products of neutron interaction with silicon. The LET of alpha particles is less than 2 MeV-cm²/mg and so the expected SET pulse width from alpha particle radiation is less than 200ps. Cosmic ray neutrons result in Si-recoil reactions in terrestrial environments. The probability of recoil reactions with energies greater than 15 MeV is negligibly small [15], so according to the results in [9] the expected SET pulse width for these environments is less than 450ps. Therefore DF-DICE cells targeted for 450ps will suffice for all terrestrial applications either at sea level or at higher altitudes. For space environments the flux of ions drastically decreases after an LET of around 60 MeV-cm²/mg. Based on the minimum value of flux for high LET values, we can assume that the probability of transients with

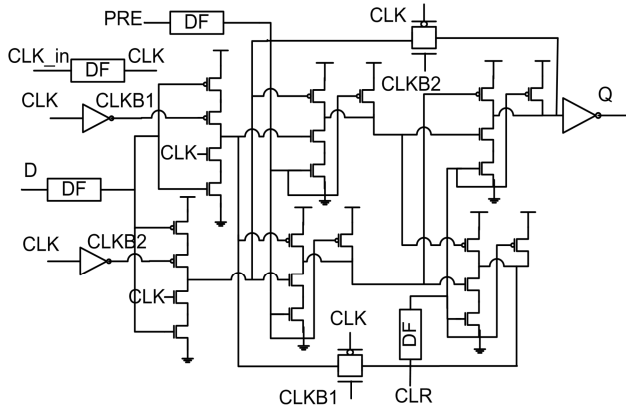


Figure 2. DF-DICE Latch

pulse widths greater than 1.2ns is negligible.

Keeping in view this range of pulse widths for the transients, we have targeted DF-DICE cells for five different SET thresholds. This scalability of DF-DICE cells for various SET thresholds is achieved by varying the number of inverters in the delay chain. A DF-DICE circuit with a particular SET threshold mitigates any transients of pulse widths less than or equal to its characteristic SET threshold. Notice that if two nodes in the storage cell are hit at the same time, the SEU immunity of the cell may no longer be effective. Also if the filter is directly hit by the incident particle then the SET immunity may be lost. In order to overcome these problems, the layout of the DICE cells should be done carefully and the filter can be implemented with some resistive hardening technique like the one discussed in [16].

IV. IMPLEMENTATION AND RESULTS

We have implemented four cells, namely: DICE latch, DICE flip-flop, DF-DICE latch, and DF-DICE flip-flop for five different SET thresholds. All the cells were laid out using the magic layout editor. The layout uses MOSIS SCMOS rules for 6-metal single poly TSMC 0.18-micron technology. The delay chain has been built using double length inverters to attain an area-efficient delay realization. The relative increase in area of DF-DICE cells against the DICE only cells has been shown in Table 1. The 3rd column shows the per-cell increase in area for DF-DICE latch and the 4th column for DF-DICE flip-flop. The performance comparison between DICE only cells and DF-DICE cells is shown in Table 2.

The per-cell results show that the increase in area can be up to 101% for 1.2ns SET threshold in a DF-DICE flip-flop. But for practical designs where sequential elements are only a part of the total area, the overall area penalty will depend on the percentage of the area occupied by sequential elements. For example, considering a practical micro-architecture design where sequential elements account for

TABLE I. AREA COMPARISON AGAINST DICE

Transient Threshold	DF-DICE latch Area (um ²)	Increase per latch	DF-DICE Flip-flop Area (um ²)	Increase per flip-flop
250ps	82160	54%	117515	31.7%
450ps	94413	77%	129768	45.5%
650ps	131936	100%	142424	59.7%
850ps	119925	124%	154878	73.5%
1200ps	145638	172%	179787	101.5%

TABLE II. SPEED COMPARISON AGAINST DICE

Transient Threshold	Increase in propagation delay	Increase in propagation delay for latch	Increase in propagation delay for flip-flop
250ps	411ps	82.2%	45.9%
450ps	598ps	119.6%	66.6%
650ps	789ps	157.8%	87.8%
850ps	973ps	194.6%	108.2%
1200ps	1342ps	268.4%	150%

30% of the total area, the relative increase in area ranges from 9.5% to 30.4% for flip-flop based designs. For the latch based circuits where area penalty per cell is higher, the area penalty ranges from 16% to 51%. The relative increase in overall area as a function of SET threshold for the above case is shown in Fig 3. Similarly, the speed penalty will depend on the operating speed of the design and on the fraction of the clock period required for sequencing overheads (propagation delays of sequential elements). For example, for a practical design running at 200 MHz frequency where the sequencing overhead is bounded by 10%, the overall reduction in speed is shown in Fig 4. It is important to realize that not all sequential elements in a design are critical for transients. So if DICE only (or ordinary storage elements) are used for the non-critical sequential elements, then the performance penalties will be further reduced. These results clearly show a linear relationship between the cost of employing DF-DICE cells and the tolerance required which in turn depends on the intended environment of operation.

V. CONCLUSION

We have proposed and evaluated latch and flip-flop designs which are tolerant not only to upsets within the storage cell but also to transients on every input signal (i.e. clock, data, preset and clear). The presented cells are scalable to various radiation environments. We have laid-out and

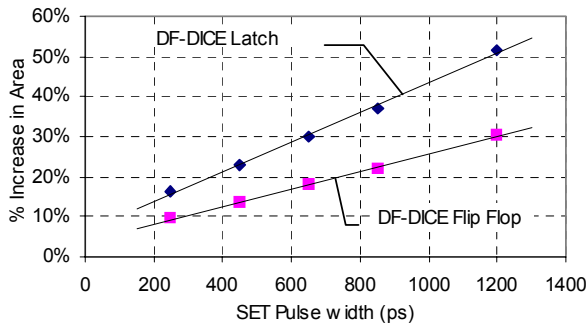


Figure 3. Overall Area Comparison

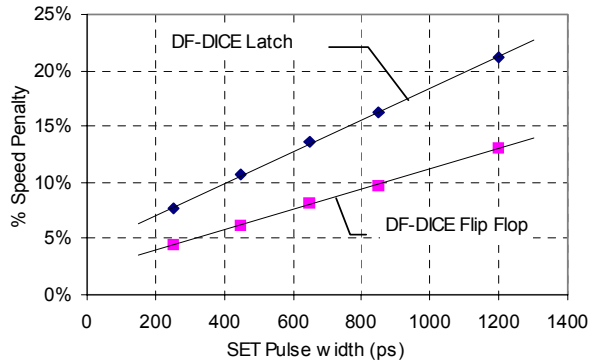


Figure 4. Overall Speed Penalty

characterized DF-DICE elements for various thresholds of SET pulse widths. The scalability analysis shows that the cost of this solution linearly scales with the required level of reliability. For a typical ASIC micro-architecture, the area penalty for flip-flop based designs is less than 30% and the reduction in speed is less than 13% for a SET threshold of 1.2ns. This design also offers a high degree of automation where all the storage elements in an existing design can be replaced with these standard cells. The design offers a soft error mitigation solution at a minimum cost for terrestrial environments and with modest cost for space environments.

REFERENCES

- [1] P. Shivakumar, M. Kistler, S.W. Keckler, D. Burger, and L. Alvisi, "Modeling the effect of technology trends on the soft error rate of combinational logic". Dependable Systems and Networks, International Conference on 23-26 June 2002 Page(s):389 – 398
- [2] T. Karnik, P. Hazucha, "Characterization of soft errors caused by single event upsets in CMOS processes". Dependable and Secure Computing, IEEE Trans on Vol 1, Issue 2, April-June 2004
- [3] D. Bessot, R. Velazco, "Design of SEU-hardened CMOS memory cells: the HIT cell". Radiation and its Effects on Components and Systems, Second European Conference on, RADECS 93, 13-16 Sept. 1993 Pages: 563 – 570
- [4] Q. Shi and G. Maki, "New design techniques for SEU immune circuits," NASA Symposium on VLSI Design, Nov, 2000.
- [5] T. Calin, M. Nicolaidis, R. Velazco, "Upset hardened memory design for submicron CMOS technology". Nuclear Science, IEEE Transactions on, Volume 43, Issue 6, Dec. 1996 Page(s):2874 – 2878
- [6] P. Liden, P. Dahlgren, R. Johansson, and J. Karlsson, "On latching probability of particle induced transients in combinational networks". Fault-Tolerant Computing, Twenty-Fourth International Symposium on 15-17 June 1994 Page(s):340 - 349
- [7] D.G. Mavis, P.H. Eaton, "Soft error rate mitigation techniques for modern microcircuits". Reliability Physics Symposium Proceedings, 40th Annual, 7-11 April 2002 Page(s):216 – 225
- [8] R. Naseer, J. Draper, "The DF-DICE storage elements for immunity to Soft Errors". Proceedings of the 48th IEEE International Midwest Symposium on Circuits and Systems, August 2005
- [9] P. Eaton, et al. "Single event transient pulsewidth measurements using a variable temporal latch technique". Nuclear Science, IEEE Transactions on Volume 51, Issue 6, Part 2, Dec. 2004 Page(s):3365 – 3368
- [10] A. Taber, E. Normand, "Single event upset in avionics". Nuclear Science, IEEE Transactions on Volume 40, Issue 2, April 1993 Page(s):120 - 126
- [11] <https://creme96.nrl.navy.mil/>
- [12] J. Benedetto, et al., "Heavy ion-induced digital single-event transients in deep submicron Processes". Nuclear Science, IEEE Transactions on, Volume: 51, Issue: 6, Dec. 2004 Pages: 3480 – 3485
- [13] P. Mongkolkachit, B. Bhuvu, "Design technique for mitigation of alpha-particle-induced single-event transients in combinational logic". Device and Materials Reliability, IEEE Transactions on, Volume: 3, Issue: 3, Sept. 2003 Pages: 89 – 92
- [14] K.J. Hass, J.W. Gambles, B. Walker, M. Zampaglione, "Mitigating single svent upsets from combinational logic". 7th NASA Symposium on VLSI Design 1998
- [15] R.C. Baumann, "Soft errors in advanced semiconductor devices – Part 1: The three radiation sources". Device and Materials Reliability, IEEE Transactions on, Volume 1, Issue 1, March 2001 Pages:17-22G
- [16] M.P. Baze, S.P. Buchner, D. McMorow. "A Digital CMOS design technique for SEU hardening". Nuclear Science, IEEE Transactions on Volume 47, Issue 6, Dec. 2000 Page(s):2603 – 2608