

Phase Measurement and Adjustment of Digital Signals Using Random Sampling Technique

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Abstract—This paper introduces a technique to measure and adjust the relative phase of on-chip high speed digital signals using a random sampling technique of inferential statistics. The proposed technique as applied to timing uncertainty mitigation in the signaling of a digital system is presented as an example; the relative phase information is used to minimize the timing skew. The proposed circuit captures the state of the signals under measurement simultaneously at random instants of time and gathers a large sample data to estimate the relative phase between the signals. By carefully premeditating the sample size, the accuracy and confidence of the result can be set to a level as high as desired. Accurately sensed value of relative phase enables the correction circuit to reduce the maximum correction error, less than half the maximum delay resolution unit available for adjustment. A pure standard cell based circuit design approach is used that reduces the overall design time and circuit complexity. The test results of the proposed circuit manifest a very close correlation to the simulated and theoretically expected results. The random sampling unit (RSU) circuit proposed for phase measurement in this paper occupies 3350 (μm)² area in 130nm technology, which is an order of magnitude smaller than what is required for its analog equivalent in the same technology.

I. INTRODUCTION

Relative phase measurement and adjustment of digital signals embedded deep inside a chip becomes extremely significant for correct functionality or optimal performance of certain systems. In data communication circuits and systems the importance of the clock-to-data correlation is magnified, and maximum timing margin can be achieved only by aligning the capturing edge of the clock at a certain point in the data eye. This can be achieved through the adjustment of the relative phase of the capturing clock with respect to data. Similarly in serializer-deserializer (SERDES) technology, multiple phases of the clock are used to launch and capture data at the SERDES. The timing uncertainties in data signaling systems are mainly categorized as skew and jitter [2]. Uncertainties due to mismatched line lengths, process variations and pin parasitics, etc, are generally time invariants for a system at given operating conditions and are

grouped together to be called “skew”. Synchronous open-loop systems tolerate the skew at the cost of performance, i.e., by low-frequency operation, whereas active closed loop systems trade area for performance gain by employing phase locked loops (PLLs) or delay locked loops (DLLs). The basic idea of an active closed-loop skew compensation is to reduce exactly as much skew as needed. It is important to note that if the operating condition of a system is not time varying, it would not require frequent adjustments and fast locking mechanisms to compensate the skew. In our previous work [3], we employed a statistical random sampling technique to observe and adjust the duty cycle of an on-chip digital signal. In this paper we show how the idea proposed in [3] can be extended to observe multiple signals simultaneously with respect to each other by observing their relative phase. The observed information is then used to minimize the timing skew in the systems where operating conditions are not changing frequently. We also show how the sample size of a random sampling observation can be premeditated to achieve high accuracy and confidence level over the measured result. The rest of the paper is organized as follows. Section II discusses some conventional ways to tackle the subject problem. The mapping of statistical estimation theory using random sampling to phase measurement of digital signals is explained in Section III. The subsequent section provides the circuit level implementation details along with a brief discussion on random clock generation. Section V shows the experimental and test results, and Section VI concludes the paper.

II. PREVIOUS WORK

Phase measurement and detection is a classic VLSI and ASIC design problem. Phase detectors (PD) and Phase/Frequency detectors (PFD) are commonly used in phase locked loops and delay locked loops [6-8]. In a typical delay locked loop (DLL), a phase detector signals the loop control circuit to increase, decrease or stop the loop delay adjustment. Similarly, in a typical PLL circuit, the relative phase of the output of a voltage controlled oscillator (VCO) with respect to the reference signal is measured by a PFD

and used as feedback to adjust the VCO's output. Soliman, et al [5] explored a design space of PDs and PFDs and categorized them with respect to their functionality and implementation perspective. The design spectrum of phase measurement and detection circuits can also be divided with respect to circuit families: (1) Analog, (2) Mixed-signal and (3) Pure Digital. This paper introduces a standard cell based pure digital approach to accurately measure the relative phase based on a unique digital signal observation technique, making the design practically portable to any process or technology.

III. THEORETICAL FRAME WORK

The proposed phase measurement design employs the random sampling technique to observe the relative phase of two signals of the same frequency. The states of the signals are simultaneously captured at the edge of this random clock. The occurrences of edges of the random clock are assumed to be completely independent of the signals under phase measurement; thus, it can capture all parts of the signals with equal probability. If the two signals have the same frequency and one is leading the other with some unknown phase difference, there are four distinct regions as shown in Fig. 1. To measure the phase difference we estimate the length of the "region A" that corresponds to a simultaneously captured value "10" of the two signals. Defining p as the ratio of the "region A" to cycle time T_{cycle} i.e. $p = t_A / T_{cycle}$, and a single trial as a simultaneously captured state of the two signals that can take four distinct values 10, 11, 01 and 00 corresponding to the four regions shown in Fig. 1, the probability of capturing a logic state "10" in a single trial would be equal to p . Now let X be the number of times "10" is captured at the edge of the random clock in a sample of n trials. From the Law of Large Numbers [1] we have:

$$\lim_{n \rightarrow \infty} \frac{X}{n} = p \quad (1)$$

The value of n is kept high and can be set to obtain a certain accuracy and confidence over the observed result. $P = X/n$ is the observed proportion of number of times state "10" is captured in a sample of n trials. The probability distribution of this proportion can closely be approximated with a Gaussian distribution, whose mean is $\mu_p = p$ and standard deviation (standard error) is $\sigma_p = \sqrt{pq/n}$ [1]. The confidence limit for p is given by the following equation:

$$p = P \pm z_c \sigma_p = P \pm z_c \sqrt{\frac{pq}{n}} = P \pm z_c \sqrt{\frac{p(1-p)}{n}} \quad (2)$$

where $\pm z_c$ is the critical value that represents the limits within which the area under the bell shaped Gaussian distribution curve is equal to the confidence interval, also known as confidence level. The value $\pm z_c$ for a desired confidence interval CI can be found by $z_c = \sqrt{2} \cdot \text{erf}^{-1}(CI)$, and its values are frequently tabulated in literature. It has been shown in [3] that for large values of n the confidence limit equation (2) can be reduced in terms of P and z_c to find

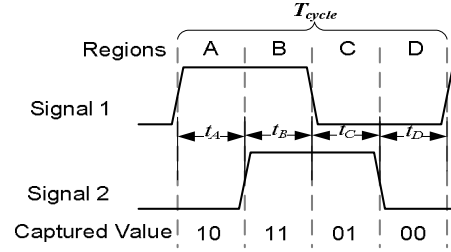


Figure 1. Two signals under relative phase measurement.

the sample size n corresponding to a certain confidence level and possible observed error $\alpha = (p-P)$ as following:

$$n = \left(\frac{z_c}{\alpha} \right)^2 P(1-P) \quad (3)$$

The observed value of P can now be mapped to relative phase using equation $\phi = 2\pi P = 2\pi \cdot t_A / T_{cycle}$ with a certain confidence and error level. It is obvious from the equation that n has a quadratic relation with accuracy. Fig. 2 shows the relation of sample size with the desired confidence level and tolerable error level for $p=0.5$ (that corresponds to maximum value of n). A \log_2 scale representation is used to directly determine an optimum size of binary counters needed for circuit implementation as described in the subsequent sections.

IV. DESIGN CONCEPT AND IMPLEMENTATION

The block diagram of a signaling convention shown in Fig. 3 explains the design concept of the proposed technique, where phase measurement and adjustment through random sampling is employed for a typical problem of placing the capturing edge of the clock in the middle of the eye of received data symbols. The circuit employs a programmable delay line at the receiver side in the path of the clock to adjust its sampling edge at a desired phase with respect to the data to be sampled. During the clock to data alignment step, a pattern of known frequency (clock itself in this case) is sent at both data and clock lines. The random sampling unit captures the state of the data and clock lines simultaneously at the edges of a random clock. The random sampling unit records a required number of observations to measure the phase difference between the signals received through the

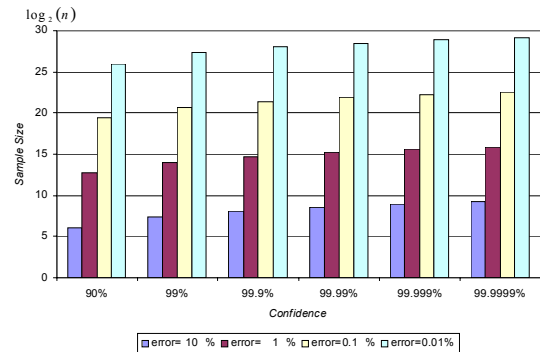


Figure 2. Sample size versus Confidence Level (at $p=0.5$).

two paths. The control unit uses the phase difference information and sets the taps of the delay line to adjust the phase of the clock with respect to the data line to provide maximum tolerance against timing uncertainties by minimizing the timing skew in the two paths.

A. Random Sampling Unit (RSU)

Theoretically the random sampling unit (RSU) consists simply of flip-flops clocked with a random clock (See Para “C”). The practical implementation of such a sampling circuit requires careful handling of metastability issues since the clock of the latching register and the input signal may switch simultaneously. The register output could settle into an un-defined region—neither a logical high nor a logical low. To alleviate this problem several solutions exist in the text [9]. Maggioni et al used sample and holds with comparators in [4]. To keep the circuits portable and purely digital we employed a simple approach that uses cascaded flip-flops to demetastabilize the sampled value of the input signal by providing it enough time to settle down to a stable value before it is consumed by other logic.

The implementation block diagram of the random sampling unit is shown in Fig. 4, it includes two event counters. At any transition of control signal “Sample”, “Counter 1” is loaded with “Desired Sample Size (n)” and “Counter 2” is reset. At every active edge of the random clock, “Counter 1” is decremented, whereas “Counter 2” is incremented only when the captured state matches with the “Region Code”, e.g., for region A, Region Code = “10”. When “Counter 1” decrements to zero, further sampling is stopped and “Counter 2” is read to calculate the phase difference of the two input signals. The size of the counters used depends upon the required accuracy and confidence level. Our design space exploration shows that a design with 16-bit counters could be implemented within a modest area (1745 cells of size $0.4\mu\text{m} \times 4.8\mu\text{m}$ in IBM Cu-11, 130nm technology) and provides 99% accuracy with a 99.9999% confidence level. To make the correction process faster, coarser measurements can be done in the beginning with smaller sized samples, and more accurate measurements can be performed with large sized samples towards the end of the correction process.

B. Phase Correction Error

Timing jitter in the signals due to power supply noise is defined to be a zero mean random variable [2]. The error induced in the phase measurement due to jitter in the signals under measurement is averaged out to zero for large sized sample, by virtue of its zero mean characteristic. The high measurement accuracy achievable through the proposed random sampling technique enables the control unit to select the delay line tap that minimizes the phase correction error due to quantization effect of the maximum delay adjustment resolution possible through the employed delay line. As an example, consider a 500 MHz system that requires a phase adjustment of 36° to eliminate skew and achieve maximum timing margin. The maximum delay resolution of the delay

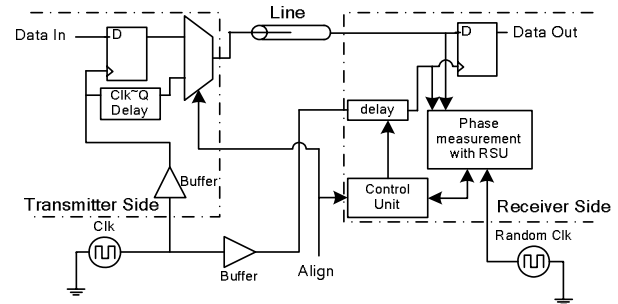


Figure 3. Digital System with Closed Loop Signaling Convention.

line in the target technology is 33ps. Ideally the clock should be delayed by 400ps, but the closest approximations can be achieved by selecting the 12th or 13th tap that yield 396ps and 429ps delays, respectively. The accurate phase measurement enables the control unit to select the 12th tap to keep the correction error to 4ps instead of 29ps.

C. Random Clock

The random clock is one of the most important components of the proposed technique. Theoretically the random clock is a signal whose edge has uniformly distributed probability of occurrence with respect to the signals under observation, so that all parts of the signals can be observed with equal probability, thus making a single observation a Bernoulli trial. Although very high quality random clocks can be generated using on-chip chaos-based circuits like chaotic oscillators [10,11] as suggested in [3], the implementation of the proposed phase measurement circuit does not necessarily require such a resource heavy on-chip random clock generator. To integrate an on-chip random clock generator we have employed a pure digital design approach as suggested in [4], as shown in Fig. 5. A linear feedback shift register (LFSR) is used to generate pseudo random numbers, which controls the length of a ring oscillator. The capricious behavioral characteristics of a ring oscillator together with a pseudo-random number generated by a LFSR produce a random clock that can be used to feed the RSU for phase measurement. Since the speed (average frequency) of the random clock has no direct bearing on the accuracy of the measurement results, this gives another dimension of flexibility in random clock oscillator design.

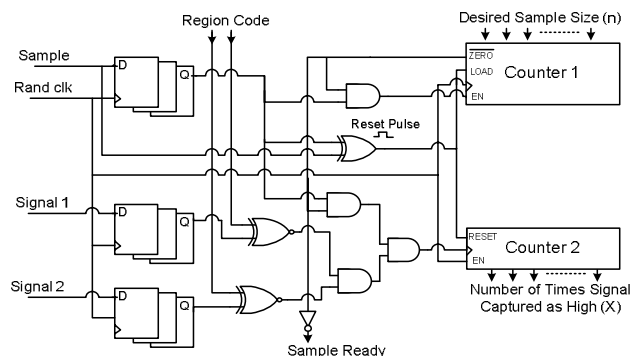


Figure 4. Random Sampling Unit (RSU) for Relative Phase Measurement.

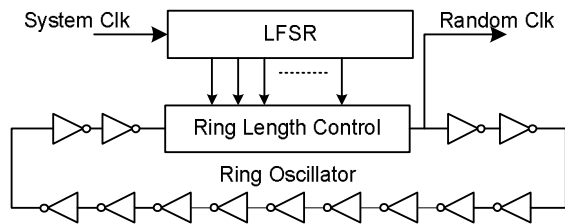


Figure 5. Digital Random Clock Oscillator.

V. EXPERIMENTAL SETUP AND RESULTS

Functional verification of the proposed technique is done through post synthesis simulations of the design targeted to IBM Cu-11 (130nm) technology. Simulation test benches used uniformly distributed random numbers to generate a random clock as stimulus for the synthesized netlist. To validate the idea for physical design, the RSU along with the integrated random clock generator shown in Fig. 5 was synthesized and ported to a Xilinx FPGA. Two periodic signals with frequency of the order of 100MHz, one of which is delayed using digitally controlled delay lines, were used to test phase measurement accuracy and consistency of RSU. Extensive series of experiments were performed for various combinations of accuracy and confidence level with input signals at different relative phase settings. The relative phase values measured with the RSU in these experiments are compared against the same observed through a digital oscilloscope. Due to space constraints only the results for signals at 90° are shown. The 90° phase difference results are chosen because in a typical double data rate digital signaling system, clock to data adjustment is kept at 90° for maximum timing margin. Moreover, the expected error level is nearly at its maximum value while observing two signals at 90° phase difference for any given sample size and confidence level. Fig. 6 shows the maximum observed error in 100 experiments run for each set of parameters over signals at 90° phase difference. The results are normalized to expected error for each case so that fine-level detail could be observed for all cases on the graph shown. The decreasing trend of observed error with increased confidence level is a consequence of increased sample size. The results show that

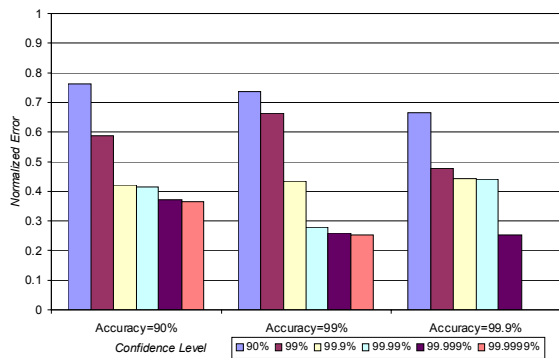


Figure 6. Maximum Observed Error Normalized by Expected Error.

the observed error is always within the limits of expected error and the proposed technique is equally valid at different accuracy settings.

VI. CONCLUSION

This paper introduces a unique idea for high-speed digital VLSI signal observation and manipulation by sensing the relative phase of multiple signals. Using premeditated parameters, a much enhanced measurement accuracy and wide range of measurements can be obtained. Measurement error due to jitter is cancelled out by the zero mean random characteristic of jitter itself. The maximum phase correction error of the adjustment circuit is reduced to half the maximum delay resolution of a delay line without involving any resource-heavy analog components or custom designed digital components. The circuit is implemented purely with standard cells, making it extremely suitable for System On-Chip (SoC) applications since it is design time efficient and portable to any process or technology. The theory of high-speed signal observation and measurement using the random sampling technique proposed in this paper is not only good for digital VLSI circuits and systems, but it can be extended to other domains of science and engineering like instrumentation, power electronics and industrial controls, etc.

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