A 50-MHZ CONTINUOUS-TIME SWITCHED-CURRENT $\Sigma\Delta$ MODULATOR

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ABSTRACT

A new architecture of second-order continuous-time switched-current $\Sigma\Delta$ modulator is presented. A Reference Current Generator is used in the second stage to solve the scaling problem. A novel current switch is designed to minimize the clock feedthrough problem and increase the operating speed. With a 50 MHz sampling rate, it has achieved 50 dB dynamic range (8-bit) at 1 MHz. This modulator has been fabricated in a 2um CMOS process with an active area of 0.37 mm^2. The power dissipation is 15 mW.

1. INTRODUCTION

Most of the recent research on high-speed low-power A-to-D conversion has focused on high-speed, high-order, multi-bit switched-capacitor $\Sigma\Delta$ modulators. However, the speed of the switched-capacitor $\Sigma\Delta$ modulator is limited mainly by the OPAMP settling time. To reduce the OPAMP settling time, the cost of increased power dissipation and larger silicon area must be paid. The use of the multi-bit $\Sigma\Delta$ modulator requires a flash A-to-D converter in the modulator, increasing the power dissipation and the modulator size.

In contrast, the continuous-time switched-current $\Sigma\Delta$ modulator can operate at high sampling speeds with much lower power consumption. It directly integrates the current onto capacitors, which eliminates the need for a high-speed OPAMP. It also has the advantage of smaller size due to simplified circuit structure and fewer capacitors. However, continuous-time switched-current $\Sigma\Delta$ modulators suffer from scaling, clock feedthrough, and clock jitter problems, which limit this kind of modulator to lower-speed or lower-resolution applications[1, 2].

In the past, the integrator gain of the continuous-time switched-current $\Sigma\Delta$ modulator has been set by the RC time constant of the on-chip resistors and capacitors[2, 3]. It was not accurately controllable due to process variation, which led to gain error of the integrator. This gain error causes scaling and stability problems and is either solved by an external compensation [3] or limits the modulator's use to first-order modulation[2].

The clock feedthrough problem has not been successfully solved. Excess charges injected from the clock through the current switches cause error on the modulator outputs. This effect must be minimized by reducing the clock speed. The operating speed of the continuous-time switched-current $\Sigma\Delta$ modulator is greatly limited by this effect.

2. CIRCUIT DESIGN

The proposed new architecture uses a fully differential design (as shown in Figure 1) to minimize the injected noise from VDD and the environment. Instead of switching between the current source and current sink, the new current switch switches only one current sink between two capacitors. It eliminates the switching time mismatch problem and the parasitic capacitance problem.

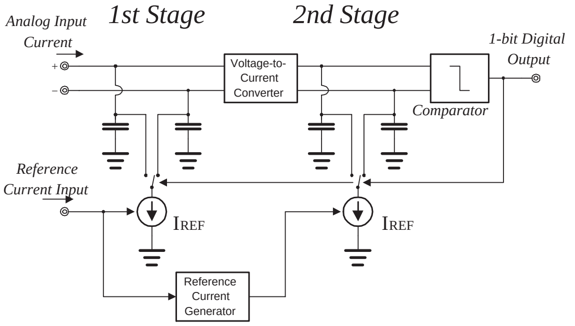

Figure 1: The architecture of the new second-order continuous-time switched-current $\Sigma\Delta$ modulator.

The purpose of the Reference Current Generator is to generate a proper reference current for the second stage, which defines the integrator gain of the first stage and hence solves the scaling problem and stabilizes the system. The circuit design of each block is described briefly in the following sections.

2.1. The Current Switch

The current switch is realized by an NMOS differential pair (M1, M2) as shown in Figure 2. The D-type flip-flops are used to synchronize the switching with the clock to guarantee each integration is exactly one clock cycle. The Common-Mode Feedback (CMFB) is a continuous-time common-mode feedback used to stabilize the common-mode voltage.

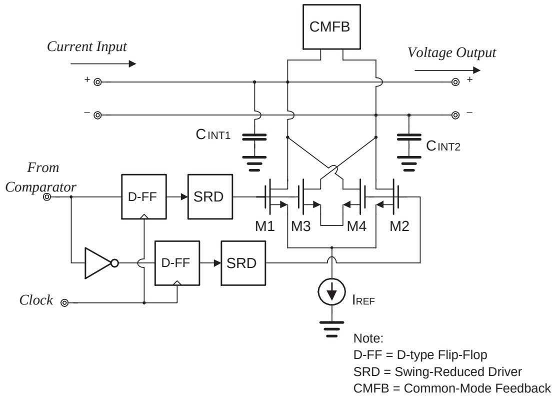

Figure 2: The simplified scheme of the high-speed current switch.

The Swing-Reduced Driver is used to reduce the voltage swing on the gates of M1–M4. This minimizes the clock feedthrough problem and also reduces the charges transferred from/to the gates, and hence, increases the switching speed. M3 and M4 are two dummy transistors with the same sizes as M1 and M2. They are used to cancel out the feedthrough charges from the gates.

2.2. The Common-Mode Feedback

The Common-Mode Feedback is a continuous-time common-mode feedback with very high loop gain to stabilize the common-mode voltage. This will also stabilize the transconductance gain of the Voltage-to-Current Converter, which is affected by the body effect. The CMFB is actually a two-stage OPAMP with the output connected to the input (as shown in Figure 3).

There are two high-impedance points (on the output nodes of each OPAMP) which introduce two low-frequency poles and cause instability. An extra capacitor (C_C) and a resistor (R_{MC}, implemented by a MOS transistor) are introduced to slove this problem. They introduce an extra-low frequency zero and a high-frequency pole to stabilize the loop.

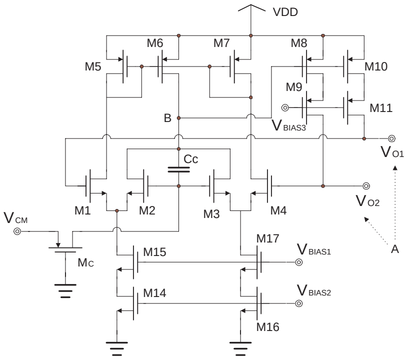

Figure 3: The circuit diagram of the continuous-time Common-Mode Feedback.

2.3. The Voltage-to-Current Converter

The Converter is realized by cross-coupled differential pairs [4]. The main differential pair composed by M1, M2, and I_{SS1} converts the input voltage into current. The other differential pair composed by M3, M4, and I_{SS2} is used to correct the linearity of the main differential pair. For optimal linearity, the ratio of transistors K_1:K_2 is set to 5:3, and the ratio of the current level I_{SS1}:I_{SS2} is set to 4:1. From SPICE simulation, the error of the linearity over the voltage input is less than 0.5%.

2.4. The Comparator

The high-speed comparator is a modified version of the comparator presented by G. M. Yin et al. [5]. It is a two-stage regenerate comparator [6] with differential cascode input stage as shown in Figure 4. The first stage is composed of M1–M5. The second stage is composed of M6–M9. M10 and M11 are used to precharge points c and d. M12 is used to reset points a and b. Φ_1 and Φ_2 are two non-overlapping clocks.

During the clock phase Φ_2, the comparator is reset. Points a and b are shorted together. When Φ_2 drops from VDD to ground, the first stage begins the regeneration process. When Φ_1 transitions high, the second stage begins the regeneration process. Either point c or point d drops to a low voltage and triggers the RS latch.

This comparator has input offset voltage and charge feedback problems. The input offset voltage problem

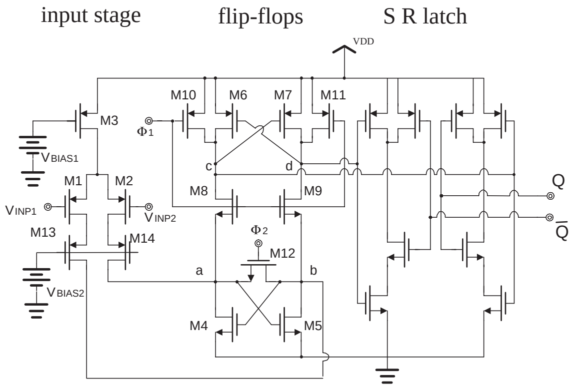

Figure 4: The simplified scheme of the high-speed current switch.

is not important for ΣΔ modulators. The charge feedback problem is solved by adding M13 and M14. During the regenerate process, some charges inject from points a and b to the two input nodes. These charges transfer to the second stage integrator capacitors and cause the error voltage. Although these charges are restored back to points a and b, an error arises in the next stage if a higher-order modulator is used. M13 and M14 are added to bypass these charges.

2.5. The Reference Current Generator

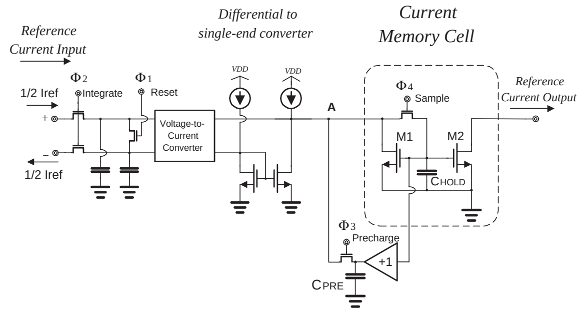

Figure 5: The simplified scheme of the Reference Current Generator.

The Reference Current Generator generates the reference current for the second stage by integrating the input reference current for two clock cycles and then holding the current level. As shown in Figure 5, the integrator is identical to the one in the first stage. A current memory cell is used to memorize (hold) the current level of the integration result. The Reference Current Generator uses four clocked states to complete the task and operates repeatedly. The four states are operated in the order S_1, S_2, S_3, S_4, and then back to S_1. Each state is two clock periods long (40 ns), and hence, the reference current of the second stage is updated every 160 ns.

The function of each state is:

- S_1 : Reset the integrator by shorting C_{INT1} and C_{INT2}.
- S_2 : Integrate the input reference current.
- S_3 : Precharge. To reduce the convergece time of the current memory.
- S_4 : Sample the current level. In this state, the current memory cell samples the output current of the integrator. After this state, the current memory cell holds this current level until the next S_1 state.

3. LOOP GAIN VERSUS STABILITY

An extra clock delay is required by the comparator and the D-type flip-flop. This extra loop delay causes a stability problem. When the scaling factor between the first stage and second stage (the integrator gain of the first stage) is greater than or equal to 0.5, the system is unstable. The two integrators tend to be saturated, which causes the modulator to settle into a long period of limit cycle and the Common-Mode Feedback to operate abnormally. As the scaling factor increases, the integrator tends to be saturated, and the input range must be reduced to avoid saturating the integrator. In contrast, a reduced scaling factor reduces the dynamic range but allows a larger input range. From extensive mathematical simulation, the scaling factor is set to 0.25 for optimal performance. The use of the Reference Current Generator ensures optimal performance and system stability.

4. EXPERIMENTAL RESULTS

The continuous-time switched-current ΣΔ modulator has been implemented in a standard 2-um N-well double-metal double-poly CMOS technology. Figure 6 shows the microphotograph. The active area of the circuit is 620×600 mm^2. With a single 5V power supply, a 50 MHz clock, and a 10 μA reference current input, it has achieved a dynamic range of 50 dB in the 1 MHz bandwidth and 70 dB in the 100 kHz bandwidth. The power dissipation is 15 mW with more than 10 mW dissipated by the digital circuitry. With a shorter channel process, the power dissipation is expected to be much lower.

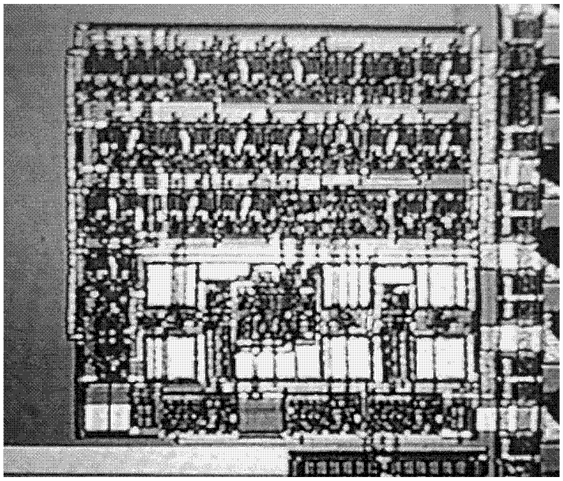

Figure 6: The microphotograph of the second-order continuous-time switched-current $\Sigma\Delta$ modulator.

Figure 7 shows a measured output spectrum with a 100 kHz input. This graph is measured by sending the modulator output directly into a spectrum analyzer. The measured noise also includes the power supply noise. The actual dynamic range may be better than this.

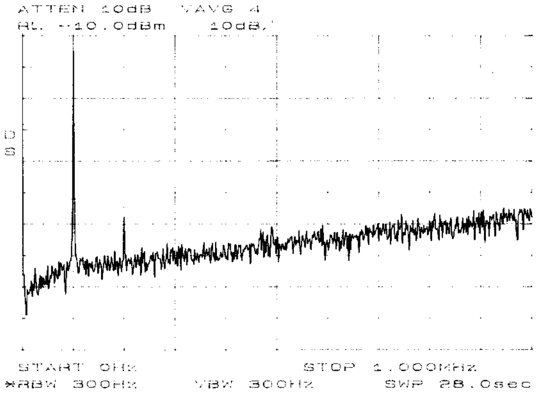

Figure 7: A measured output spectrum with a 100KHz input signal.

5. CONCLUSION

A new architecture of continuous-time switched-current $\Sigma\Delta$ modulator has successfully solved the scaling problem. The novel current switch design enables the modulator to operate at high speed with low power dissipation. The new architecture offers a low-cost way to implement a high-speed, low-power, and small-size A-to-D converter.

Table 1: Measured modulator performance

Power supply voltage	5V
Clock frequency	50MHz
Signal Bandwidth	1MHz
Dynamic range	50 dB
Input reference current	10 μA
Input current range	$\pm 5\mu$A
Power dissipation	15 mW
Active area	0.37 mm^2 ($620 \times 600\mu$m)
Technology	2μm CMOS

Acknowledgements

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