

THE DF-DICE STORAGE ELEMENT FOR IMMUNITY TO SOFT ERRORS

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Abstract—This paper describes the delay filtered dual inter-locked storage cell, which is immune to single event transients on any of the inputs and single event upsets within the storage cell. The increase in area and speed of an Application Specific Integrated Circuit (ASIC) employing the proposed cells are proportional to the targeted Single-Event Transient (SET) pulse-width. A standard ASIC can easily be converted to a soft-error tolerant design by simply replacing all the storage elements with the proposed cells. The area and speed performance of the proposed cells targeted for an 800ps wide SET have been evaluated. The resulting designs are immune to soft-errors with acceptable area penalty and modest degradation in speed.

I. INTRODUCTION

The radiation environment in space significantly affects the performance and functionality of space-borne electronic devices. In deep sub-micron technologies, even alpha particles from packaging material may result in soft errors (also known as Single Event Upsets - SEUs) [1]. The impact of radiation has historically been categorized into two groups: one reflects the effects over a long period of time, termed as Total Ionizing Dose (TID) and the other, known as single event effects (SEE), is the immediate result of a single radiant charged particle, whether from heavy ions in space or alpha particles from packaging material. Traditionally space electronics, where radiation hardening is essential for reliable operation, were manufactured at designated foundries employing specialized processes to improve the radiation tolerance of electronic devices. This method of attaining system reliability has been known as radiation hardening by process. With the changing economy of the space electronics market, these processes began losing ground due to their very high cost and poor performance because they usually lag the commercial processes by two generations. This has led to the development of Radiation Hardening by Design (RHBD) in which architecture, circuit, and layout techniques are used to mitigate radiation effects. Special layout structures, like edgeless transistors and guard-bands [2] and a new NMOS layout structure [3], are used to minimize the inter-device leakage currents and improve TID tolerance. On

the other hand, spatial and temporal redundancy is employed to mitigate SEU and Single Event Transient (SET) effects [4]-[8]. Thus RHBD trades off circuit performance (area, speed and power) for increased system reliability.

The ever decreasing thickness of gate and field oxides minimizes the trapped charge storage and results in improving the TID tolerance of commercial devices. Lower supply voltages have resulted in minimizing the latchup effects.

Although the TID hardness of new technologies is improving, Single Event Effects are becoming increasingly pronounced [9], [10]. Over the years, several solutions have been presented to overcome SEU in storage elements [4]-[7]. With increasing circuit speeds and lower driving currents, Single Event Transients occurring in combinational logic (having pulse width on the order of 350ps to 1.3ns [11]) are becoming a more important detractor for system reliability. These transients are able to propagate several gates and can be latched incorrectly in a memory element resulting in SEU. There are very few solutions presented to suppress these transients. A Temporal Latch [8] solution mitigates SETs as well as SEUs. This solution suffers from large area and power penalties since it uses Triple Modular Redundancy (TMR). A novel delay based filtering technique to mitigate SETs on a data signal input has been presented in [12] but SET mitigation on clock and other control signals and SEU mitigation within storage elements are not addressed.

In this paper, we propose to combine the above mentioned delay filtering technique with Dual Inter-locked Storage Cell (DICE) [7]. We apply this filtering technique to all the inputs of the storage cells. This design results in a highly robust digital system which is tolerant to both SETs on any of the inputs of a sequential element, including Clock, Preset, Clear and Data, and SEUs within the storage elements. We call this design the “Delay Filtered DICE (DF-DICE)”.

The area and speed of the proposed solution, which tolerates an 800ps wide SET pulse, have been evaluated. Compared to the DICE, the area penalty of the proposed

latch is 76% while that of the flip-flop is 45%. For a typical Application Specific Integrated Circuit (ASIC) having 30% of its area occupied by flip-flops, the overall chip area penalty will be less than 13.5%. The speed penalty of the proposed cell depends on the tolerance desired. For an 800ps wide SET it is around 150% for a Flip-flop. There is no need for a complex clocking scheme as required by the temporal latch design. This design offers the advantage of being easily implemented in a computer added design (CAD) flow whereby each existing storage element is simply replaced by the DF-DICE.

The remainder of the paper is organized as follows: section 2 summarizes the previous work; section 3 describes the circuit for the new cells. In section 4, we present and discuss experimental results. Section 5 concludes the paper.

II. PREVIOUS WORK

Soft error mitigation techniques involve either spatial or temporal redundancy. The simplest spatial redundancy method, triple modular redundancy (TMR), replicates critical circuit nodes (latches and flip-flops) three times and then a majority vote is used to ignore any corrupt value. This method suffers from large area and power penalties in the replicated logic and voter circuits but the speed degradation is minimal. Only the voter circuit affects the critical path for speed. This method suffers from another drawback in that it does not correct the error; instead it just forwards the correct value. The second class of spatial redundancy mitigation techniques replicates the critical nodes (latches and flip-flops) and uses feedback to recover the correct value after an upset.

The most commonly used SEU immune cells based on the above technique include the Heavy Ion Tolerant (HIT) cell [5], the Dual Interlocked Storage Cell (DICE) [7], and the Single Event Resistant Topology (SERT) cell [6]. The HIT cell suffers from the drawback that the transistor sizes are critical in restoring the correct value after a single event upset. The DICE and SERT cells do not depend on optimal transistor sizing. Both DICE and SERT offer a comparable area solution, yet the DICE cell has been widely used in industry, and sufficient data is available in the literature about the SEU immunity of the DICE cell [13].

Temporal redundancy techniques are characterized by sampling the input data at different time intervals greater than the width of the transients to be tolerated and then voting the corrupt value out. The Temporal latch [8] solution is based on this principal. It uses four clocks to sample data at different time intervals. It employs TMR to store temporally sampled values in three different latches and then uses a majority vote to forward the correct value. This design offers mitigation not only to SEU but also to SETs on data inputs. Although a modified version of this latch can mitigate SET on clock inputs, this technique fails in case of transients on asynchronous control signals like clear and preset for latches. Tripling the hardware and including the voter circuit

significantly increases the area and power overhead. Furthermore, this design suffers from a large speed penalty which is at least equal to twice the targeted SET pulse width.

A novel single event transient filtering technique for a data input signal has been presented in [12]. The basic principle is the same as temporal filtering, but the filtering action is achieved using a C-element as shown in Fig. 1. The C-element is a state holding element, and it has the basic property that it changes its output only when all the inputs are of identical logic value. The incoming data signal is fed to the C-element using two paths; one with zero delay and the other with a critical delay of $T_{critical}$ (equal to the SET pulse width to be suppressed). Hence a transient of $T_{critical}$ width will not be able to change the output of the C-element. The results show that the area overhead is negligible while the speed penalty is dependent on the transient width to be tolerated.

III. THE DELAY FILTERED DICE

The proposed circuit, shown in Fig. 2, is a combination of the delay filtering technique presented in [12], and the DICE cell described in [7]. Since transients can occur on any of the inputs to a storage cell and may result in SEU, all inputs of the storage cell are critical. Therefore, the delay filtering technique to mitigate SET is used for every input to the storage cell. We have used a clocked inverter DICE latch and flip-flop having preset and clear control signals. Fig. 2 shows only a latch version of the proposed cell. There are four delay filters on the left side, each for Clock, Data, Preset and Clear inputs. On the right side is the DICE storage latch. Since the C-element in the delay filter is inverting, an inverter is used at the output of each delay filter to restore the polarity of the input.

The operation of the circuit is as follows: The incoming clock and data signals (as well as the preset and clear control

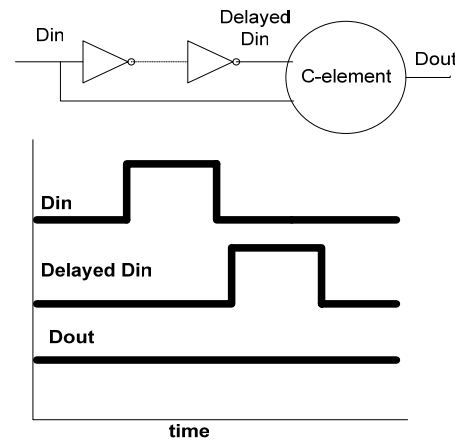


Figure 1. Delay Filter Operation

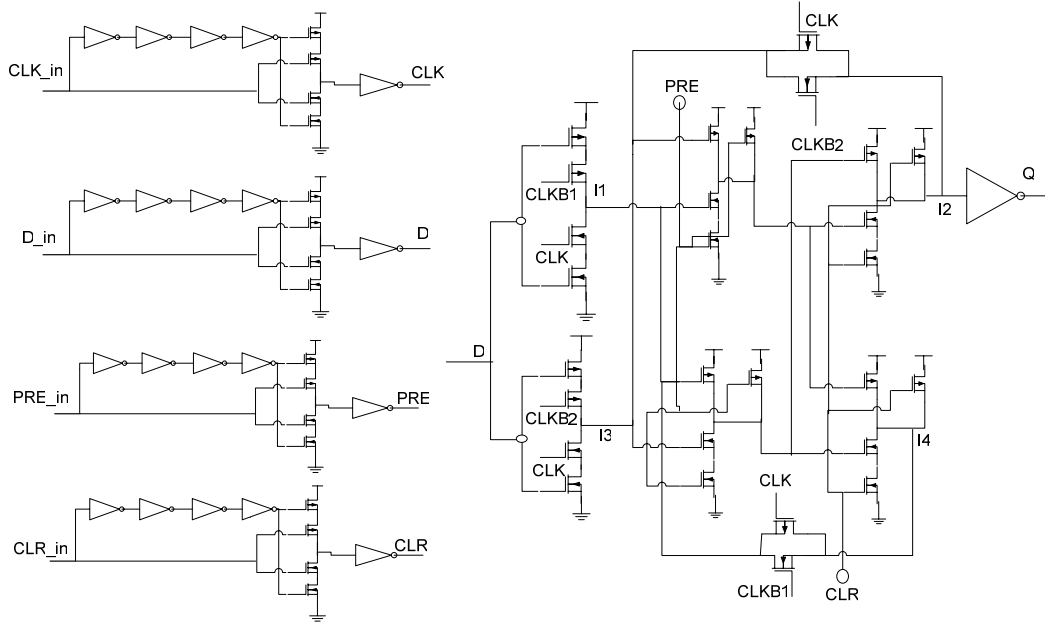


Figure 2. Delay Filtered DICE Latch

signals) pass through the delay filter. The output of the C-element will not change unless both inputs have the same logic value. Hence data and clock signals will need to be held stable for a period at least equal to the delay of the inverter chain.

As the output of the C-element is a dynamic node, it can lose its state if left floating for longer times. To overcome this problem, a weak inverter (not shown) which provides feedback and maintains the output state can be used at the output node.

If the delays of the clock and data signal through the delay filters are matched, then the setup and hold times of the internal storage cell (DICE Latch/flip-flop) will remain unchanged. However, due to the property of the delay filter, the input signals cannot transition faster than the delay of the filter. Therefore, the maximum achievable clock frequency is reduced in proportion to the targeted SET pulse width.

In the latch portion, CLKB1 and CLKB2 are the inverted version of the CLK signal. Nodes I1, I2, I3, and I4 have the same value stored in the normal latching mode. Consider a SEU, in which node I1 gets flipped from 1 to 0. The correct value at I3 will restore I1 via I4 feedback. The stored value of 1 at I3 does not allow the value of I2 to be changed either. So in the case of a SEU at a single node, the spatial redundancy and the feedback at two points restores the uncorrupted value on all the latch nodes.

IV. IMPLEMENTATION AND RESULTS

We have implemented the four cells, namely: DICE latch, DICE flip-flop, DF-DICE latch, and DF-DICE flip-

flop. All the cells were laid out using the magic layout editor. The layout uses MOSIS SCMOS rules for 5-metal single poly TSMC 0.25-micron technology. The delay chain was built using double length inverters to attain an area-efficient delay realization. A sample layout of the DF-DICE latch is shown in Fig. 3. Table 1 shows the respective areas for the cells. Since the transistor sizes were not optimized, the delay through the delay filters is different for different signals depending upon the load and wire lengths. Table 2 shows the actual delay values for the delay filters. The relative speed performance is shown in Table 3.

As shown in the results, the area penalty just considering the cells is from 45% to 76%. Considering a practical micro-architecture design, this penalty may not result in a large overall penalty, depending on the number of storage elements in the system. For example, if an ASIC has 30% of its area occupied by flip-flops, the overall chip area penalty will be less than 13.5%.

SPICE simulation results show that pulse widths of up to 825ps are actually mitigated. Looking at the speed penalty, we observe that the propagation delay for input signals increases 150%. Propagation delays for sequential elements are typically 10% of the critical path in a standard ASIC.

TABLE I. AREA COMPARISON

	DICE Cell (λ^2)	DF-DICE (λ^2)	%age increase
Latch	248x266	248x470	76%
Flip-Flop	264x444	264x646	45%

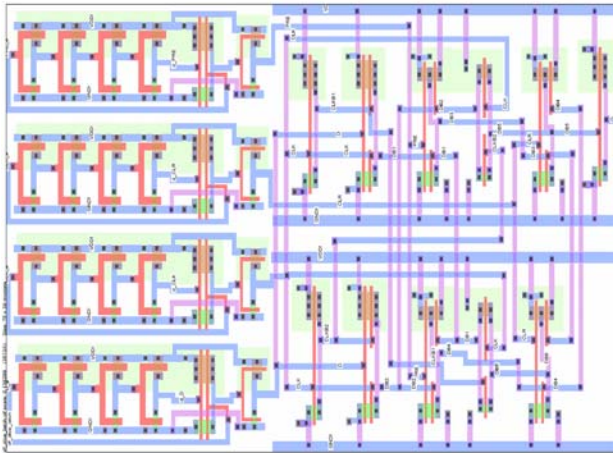


Figure 3. Layout of DF-DICE Latch

TABLE II. PROPAGATION DELAY OF FILTERS

	Delay in Data	Delay in Clock	Delay in Pre	Delay in Clear
DF-DICE Flip-flop	1080ps	1250ps	1180ps	1160ps
DF-DICE Latch	1075ps	1150ps	1080ps	1075ps

TABLE III. INCREASE IN PROPAGATION DELAYS

	Flip-flop (T _{DQ} rise)	Flip-flop (T _{DQ} fall)	Latch (T _{DQ} rise)	Latch (T _{DQ} fall)
DICE	1123ps	1450ps	697ps	725ps
DF-DICE	2144ps	2481ps	1775ps	1896
change	91%	71%	154%	161%

Therefore, for a 200MHz clock, for example, the overhead in speed is 14%. It should be noted that the circuit was targeted for a single event transient pulse width of 800ps. If the target is less than that, the speed penalty will be lower.

V. CONCLUSION

We have proposed and evaluated latch and flip-flop designs which are immune not only to transients on every signal (i.e. clock, data, preset and clear) but also to upsets within the storage cell. For typical ASIC micro-architectures, the proposed design will incur an area overhead of less than 13.5%. The speed performance of the design is directly proportional to the pulse width of the single event transients targeted. This design also offers a high degree of automation where all the storage elements in an exiting chip design can

be replaced with these standard cells. The presented technique is also helpful in improving system reliability against soft errors for ground systems.

However, note that if two nodes in the storage cell are hit at the same time, the SEU immunity of the cell will no longer be effective. Also, if the pulse width of a SET is larger than the delay in the filter, it can result in a SEU provided it occurs during the setup and hold time window at the storage node. Therefore, an effective estimation of the transient pulse width in a particular environment is necessary before finalizing the design decisions.

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