

# A THERMAL EVALUATION OF INTEGRATED CIRCUITS: ON CHIP OFFSET TEMPERATURE MEASUREMENT AND MODELING

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## Abstract

**This paper presents a chip and test configuration for thermal evaluation based on MOSIS 0.5 $\mu$  technology. We measured spatial temperature differences as high as 20.65°C on a 2mm by 2mm Tiny Chip. Our research shows that circuit location on a chip determines its default offset temperature and heat transport properties, which must be considered for prediction of junction temperature and electro-thermal analysis. A model has been developed to verify measurement results. The results yield insight about on-chip heat dissipation, which is very useful for mixed-signal VLSI designs and circuit reliability analysis.**

## I. Introduction

On-chip thermal distribution and local heat-up is an important factor in high-speed VLSI design and MCM (Multi Chip Module) systems. Much research has focused on the predictions of junction temperature and power generation in circuits [1-3]. Recent approaches have combined thermal transport properties to get more precise predictions [4-7]. Meshing [8], finite element analysis and thermal circuits [9] are popular methods to simulate thermal transport properties. However, meshing and thermal circuits introduce some difficulties. For instance, different meshing approaches or thermal circuit models generate different results for the same circuit, often differing by as much as two orders of magnitude in thermal transport properties. Furthermore, these methods tend to involve intricate mathematics, and the solutions are often elusive.

In this paper we present a chip and its testing configuration. A chip was designed to measure the spatial temperature differences. Using the special

floor plan and circuit modules, we are able to simplify the thermal transport properties to develop and verify heat transportation conditions and models. The design, configuration for calibration and testing are described in Section II.

In Section III, we present an analytical model based on general heat source setup and heat transfer assumptions. Applying differential equation theories, we achieve a set of continuous equations, which describe the thermal transport properties on each point of a die. The model provides clean, simple analytical solutions of heat dissipation conditions, which yield the offset temperature for junction-temperature estimation and on-chip thermal distribution predictions. We describe assumptions and justification for the assumptions, as well as the derivation and results.

Along with the design and modeling, we present the measured results in Section IV. Both theoretical and measured results are discussed here. The utility of the spatial and temporal results are discussed, and potential improvements are also addressed.

## II. Design and Configuration

The goal of this design is to measure the spatial temperature differences on chip. We use five circuit modules in a spiral floor plan to produce a variety of combinations of heat sources and sensors. Each module contains a pad driver, a poly-silicon resistor, and a diode. The pad driver is used as the heat source. Poly resistors and diodes function as temperature sensors. A picture of the chip layout is shown in Figure 1. The chip was designed and fabricated using a MOSIS 0.5 $\mu$  process.

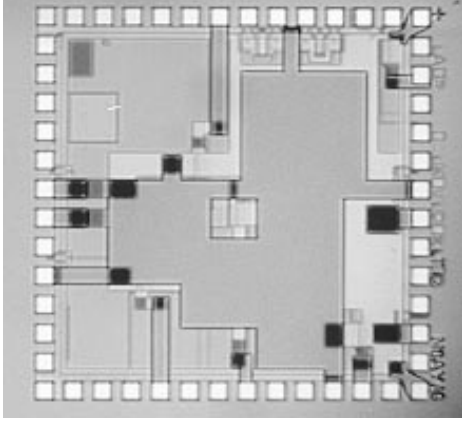


Figure 1. Microscope Picture of the test chip (The spiral layout shows from the center to the border, they are PAD1, PAD2, PAD3, PAD4, PAD5 respectively.)

Each pad driver is considered a point heat source since it occupies less than 1% of the chip area. Several researchers have verified the accuracy of using diodes and resistors as on-chip thermometers [10,11]. Here we use non-silicide polysilicon resistors, which are provided in the MOSIS 0.5 $\mu$  process.

The diodes and resistors were calibrated using a thermal bath with a thermal chamber and test board. After the calibration, we applied linear regression to get the algebraic expression and lookup table for the thermometers.

With the above setup and calibration, we measured different combinations of heat source and thermometers. With different combinations of variables, we are able to measure spatial temperature differences. One set of experiments was conducted with a fixed heat source location and varying sensor locations. Another set was conducted with a fixed temperature sensor location and varying heat source locations. Both experiment results and comparison to the model are shown in Section IV.

### III. Model Development

The goal of our model is to develop a set of equations to calculate the temperature distribution regarding geometry and time. We define a chip with a periodic heat source applied in the center of the upper face. The heat transfer on five sides of the chip

(upper side and surrounding four sides) are modeled as adiabatic processes, while the bottom side attached to the package is modeled as an isothermal process. Therefore, heat will dissipate from the center to the package. This assumption is based on the packaging style of most die. The five adiabatic sides have a die to air interface, which has negligible heat transfer compared to the die-package interface. The bottom side is isothermal, because the package is assumed adequate for dissipating heat immediately from the die to the outside environment.

Using the above assumptions as the boundary conditions, and solving using partial differential equation theory, we get the following results.

Define the temperature function as

$$u(x, y, z, t) \text{ with } x, y, z \in \Gamma, t > 0$$

$$\Gamma = \left\{ (x, y, z) \mid -\frac{L}{2} \leq x \leq \frac{L}{2}, -\frac{L}{2} \leq y \leq \frac{L}{2}, -w \leq z \leq 0 \right\}$$

Where  $t$  is time,  $\Gamma$  is the geometry of the die,  $x, y, z$  represent the coordinates,  $L$  is the length of the edge of the die, and  $w$  is the thickness of the wafer.

Assume there is a unit heat source placed at the point  $(0, 0, 0)$  at  $t=0$ . We want to know the temperature distribution of  $\Gamma$  at any given moment for  $t > 0$ .

The boundary condition is prescribed by a Neumann problem (adiabatic) on 5 faces of  $\Gamma$  other than the bottom face, and a Dirichlet (isothermal) problem on the bottom face. From partial differential equation theory, we know this problem has a unique solution for  $u$ . Therefore, we obtain the following thermal distribution function as (1).

Finally, we compute the case when there are unit heats added to the origin periodically. The temperature distribution function,  $u_{\infty}(x, y, z, t)$  is a periodic function after infinite unit heat sources are added. We obtain the thermal distribution function(2).

With the above equations (1)(2), we are able to predict and verify the temperature differences and estimate the temperature variant according to time. The numerical results are shown in the next section.

$$u(x, y, z) = 8 \left[ \sum_{k=0}^{C_{ut}} e^{-\frac{4k^2\pi^2t\gamma}{L^2}} \cos\left(\frac{2k\pi x}{L}\right) \right] \times \left[ \sum_{k=0}^{C_{ut}} e^{-\frac{4k^2\pi^2t\gamma}{L^2}} \cos\left(\frac{2k\pi y}{L}\right) \right] \times \left[ \sum_{k=0}^{C_{ut}} e^{-\frac{(2k+1)^2\pi^2t\gamma}{4w^2}} \cos\left(\frac{(2k+1)\pi z}{2w}\right) \right]$$

where  $\gamma = \frac{K}{\rho \times C_p}$ ,  $K$  is the thermal conductivity,  $\rho$  is density, and  $C_p$  is heat capacity of silicon. (1)

$$u_{\infty}(x, y, z, t) = \sum_{\tau=0}^{\infty} u(x, y, z, t + \frac{\tau}{f}) \quad , \text{ where } 0 < t < \tau, f \text{ is the frequency}$$

$$\Rightarrow u(x, y, z, t) = \sum_{\tau=0}^{\text{time}=\infty} 8 \left[ \sum_{k=0}^{\text{Cut}} e^{\frac{-4k^2\pi^2(t+\frac{\tau}{f})\gamma}{L^2}} \cos\left(\frac{2k\pi x}{L}\right) \right] \times \left[ \sum_{k=0}^{\text{Cut}} e^{\frac{-4k^2\pi^2(t+\frac{\tau}{f})\gamma}{L^2}} \cos\left(\frac{2k\pi y}{L}\right) \right] \times \left[ \sum_{k=0}^{\text{Cut}} e^{\frac{-(2k+1)^2\pi^2(t+\frac{\tau}{f})\gamma}{4w^2}} \cos\left(\frac{(2k+1)\pi z}{2w}\right) \right] \quad (2)$$

#### IV. Results

Substituting the geometry, power and frequency of our test chip into the model, we achieved the following temperature plot for the top surface of the die.

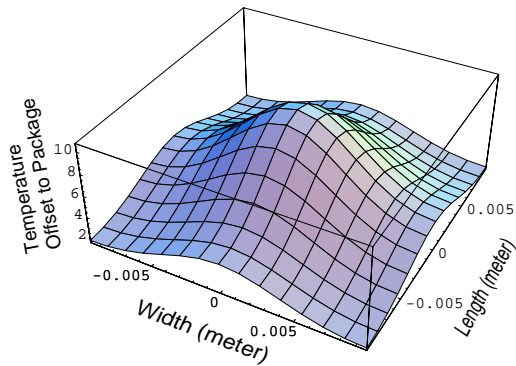


Figure 2. The temperature distribution on die's surface, the heat source is located in the center, z-axis represents relative temperature difference( $^{\circ}\text{C}$ ), x,y represent location on the surface(m).(k=20)

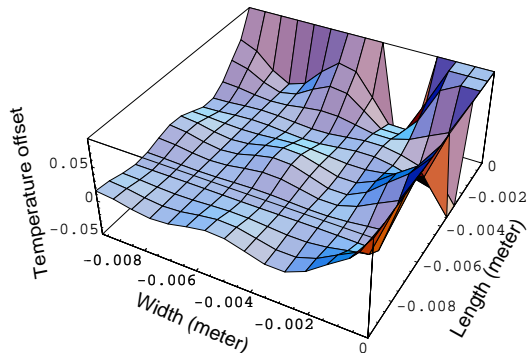


Figure 3. The temperature on the quarter of die surface. z-axis represents relative temperature difference( $^{\circ}\text{C}$ ), x,y represent location on the surface(m), (k=200)

Figure 2 and Figure 3 are plots from equation(2). Using a small  $k$ , we can achieve the equilibrium temperature to verify the temperature offset from the measurement.

With a larger  $k$  value for the infinite series,(k=200 for Figure 3), we obtain the ripple style temperature surface which is due to the periodic heat

source. The swing on the surface of the chip will be  $0.02^{\circ}\text{C}$  where outside the heat source area.

Figure 4 shows the temperature dropping curve in the heat source location. This result shows a temporal temperature difference of  $450^{\circ}\text{C}$  in transistor junctions. The temporal varying of temperature is significant in limited geometry and cannot be neglected in electro-thermal simulations.

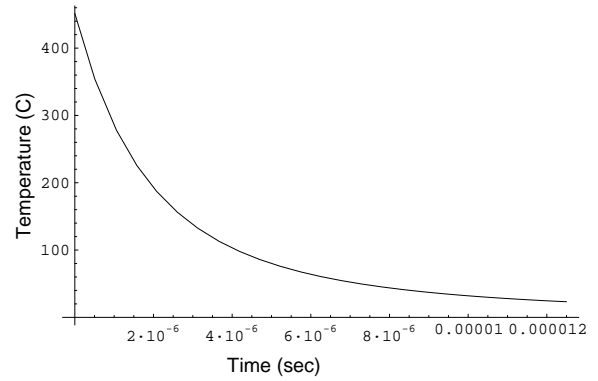


Figure 4. Temperature drop in heat source from the model.

#### Fixed Heat Source Location Experiments

The spatial temperature differences from our measurement and model are shown in the following table. As shown in the table, the measurements agree within 13% of the model for non-negligible temperature offsets. Figure 5 shows the temperature readings from the measurement.

	Model	Measurement
Pad1	9.25	10.52
Pad2	14.58	15.50
Pad3	1.15	2.24
Pad4	0.01	0.00
Pad5	0.00	0.00

Table1. Comparison of spatial temperature differences from model and measurement.

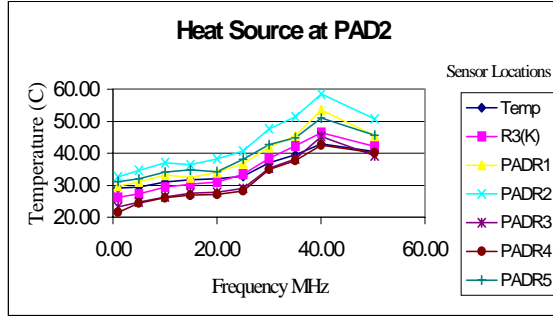


Figure 5. Spatial temperature offset from measurement.

### Fixed Sensor Location Experiments

In Table 2, we have measured PAD1's temperature while varying the location of the heat source among PAD2-PAD5. As shown in the data, we achieved a temperature difference of 20.65°C between 0.556W applied at PAD5 versus PAD2. These results show that the spatial temperature offset generated by different locations is significant.

Circuit Frequency	Heat Source Locations				
	Pad2	Pad3	Pad4	Pad5	All Pads
1.00	29.72	31.90	31.94	29.99	34.11
5.00	30.96	31.35	31.39	30.26	36.49
10.00	33.18	31.00	31.55	31.74	39.05
15.00	32.40	33.26	33.61	30.65	42.82
20.00	33.96	31.78	34.81	32.67	41.89
30.00	41.89	33.92	34.62	34.39	48.77
40.00	53.52	36.37	35.44	32.87	59.39
50.00	45.55	39.13	36.02	33.84	61.14

Table 2. PAD1 temperature with different heat source

Our theoretical model indicates the center location has the worst condition for heat dissipation, while the border of the chip has the best condition. When we apply the same amount of heat in different locations on the chip, we see significant temperature differences on the chip as well as the package.

In Figure 6, we also measured the package temperature while varying the heat source location. There is a 13.40°C difference between a heat source applied at the center versus the border. This result matches our prediction in the model and also confirms that different heat dissipation due to location on the chip is not negligible.

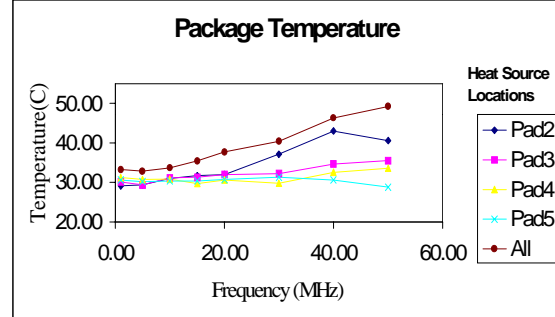


Figure 6. Package temperature.

From the above results, we measured spatial temperatures. Our theoretical models also verified the measurements. The results verify our prediction of the thermal characteristics on the chip and show that heat dissipation assumptions in our model are correct. The model is precise and closely matched our measurement results.

Our models also predict the temperature variation in very small amounts of time and show that temporal variations are significant, possibly influencing circuit behavior. A meaningful direction for future work is to attempt to measure this temporal behavior in a test configuration.

### V. Conclusion

This paper presents and illustrates the combination of measurement and modeling of thermal distribution for integrated circuits. The quantification of spatial and temporal temperature offsets show that local heat-up cannot be neglected, especially for mixed-signal integrated circuits, multi-chip modules and circuit reliability analysis. A model has been provided to explain the temperature differences due to location and geometry. Such measurement results and models provide insight into heat dissipation, which is necessary for transient electro-thermal analysis, junction temperature prediction and on-chip thermal management systems to achieve a more accurate result.

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## Reference:

- [1] C. S. Dake Liu, "Power Consumption Estimation in CMOS VLSI Chips," *IEEE Journal of Solid State Circuits*, vol. 29, pp. 663-670, 1994.
- [2] R. B. C. Lallement, T. Maurel, "Modeling of Power Mosfet and Bipolar Transistors Taking Into Account the Thermoelectrical Interactions," in *Modeling in Analog Design*, vol. 2, *Current Issues in Electronic Modeling*, O. L. Jean-Michel Berge, Jacques Rouillard, Ed. Dordrecht: Kluwer Academic Publishers, 1995, pp. 121-143.
- [3] M. H. Ricardo Gonzalez, "Energy Dissipation In General Purpose Microprocessors," *IEEE Journal of Solid-State Circuits*, vol. 31, pp. 1277-1284, 1996.
- [4] A. M. R.P. Tye, "Determination of Appropriate Thermal Transport Properties for Electronics Applications," presented at 8th IEEE SEMI-THERM Symposium, 1992.
- [5] C. J. M. L. H. Vinke, "Recent Achievement in the Thermal Characterization of Electronic Devices by Means of Boundary Condition Independent Compact Models," presented at 13th IEEE SEMI-THERM Symposium, Austin, Texas, 1997.
- [6] J. W. Sofia, "Analysis of Thermal Transient Data with Synthesized Dynamic Models for Semiconductor Devices," presented at 10th IEEE SEMI-THERM, 1994.
- [7] E. C. H.A. Mantooth, "Modeling and Simulation of Electrical and Thermal Interaction," in *Modeling in Analog Design*, vol. 2, *Current Issues in Electronic Modeling*, O. L. Jean-Michel Berge, Jacques Rouillard, Ed. Dordrecht: Kluwer Academic Publishers, 1995, pp. 93-120.
- [8] G. J. Luc Hebrard, Bernard Boutherein and Michiel Le Helley, "Simulation of Electronthermal Interaction in Power Integrated Circuits," presented at 8th IEEE SEMI-THERM Symposium, 1992.
- [9] H. V. Clemens Lasance, Harvey Rosten, Karl-Ludwig Weiner, "A Novel Approach for the Thermal Characterization of Electronic Parts," presented at 11th IEEE SEMI-THERM Symposium, 1995.
- [10] H. S. Alan Claassen, "Comparison of Diodes and Resistors for Measuring Chip Temperature During Thermal Characterization of Electronic Packages Using Thermal Test Chips," presented at 13th IEEE SEMI-THERM Symposium, Austin, Texas, 1997.
- [11] H. Shaukatullah, "A Method of Using Thermal Test Chips With Diodes for Thermal Characterization of Electronic Packages Without Calibration," presented at 11th SEMI-THERM Symposium, 1995.