

**Syllabus**  
**EE 327x — Digital Electronics**  
**Department of Electrical Engineering, University of Southern California**  
**Spring 2005**

**Content**

EE 327x serves as an introduction to the devices, processes, and design techniques used to implement digital circuits in very large scale integrated systems, and is a gateway for students who are interested in modern implementations of computer hardware.

**Administration**

The prerequisite for EE 327x is EE 326Lx (Essentials of Electrical Engineering), and credit is limited to CECS majors (others by instructor permission). The course is taught in a studio format in which lecture, discussion, computer, and laboratory activities are combined in the same setting. Weekly sessions meet on Tuesday and Thursday from 12:30 to 1:50 in OHE 230.

**Grade**

The grade for EE 327x is determined by the following weighted components:

First midterm examination	20%
Second midterm examination	20%
Homework	15%
Comprehensive design project	15%
Final examination	30%

Students who are absent on the date of a midterm examination will receive a score of zero unless excused by the instructor **prior to the exam**, in which case the final exam score will replace the missing midterm exam score. Bring your USC ID card to each exam. **Make-up exams (midterms and final) will not be scheduled.**

Incomplete grades (IN) are assigned only in exceptional cases.

**Homework**

Homework will be assigned during class and will be due at the **beginning** of the class session on the due date. Homework is not accepted after the due date. The two lowest homework grades will be dropped from the total used for computing the course grade. Homework assignments are intended to provide essential practice in the fundamentals of digital integrated circuit design, and their value as preparatory exercises for the midterms and final examinations should not be underestimated. Note also that the strength of a student's performance on homework may tip the balance when that student's overall score for the course lies between two letter grades.

**Design Project**

A comprehensive design project will be assigned approximately four weeks before the end of the term and will be due on the last day of class. Students may work in teams of two or three. The contributions of each team member must be acknowledged in each student's project report, and each team member must be prepared to explain any aspect of the design.

**Attendance**

Lectures and classroom discussion provide indispensable integration of the specific details and general principles covered in each topic. Homework and examination problems may be drawn from material covered in class meetings which is not addressed in the assigned readings. Students who miss a session should obtain from a classmate any materials or course information that may have been distributed on that day.

### **Academic Integrity**

Students who cheat during an exam or on homework will receive a grade of F in the course and will be reported to the appropriate University authority for further disciplinary action.

Standards for academic integrity published in the SCampus (USC Student Guidebook, Section 11; <http://www.usc.edu/dept/publications/SCAMPUS/gov/gov05.html>) will be strictly enforced. All students are responsible for familiarity with USC rules for academic honesty and behavior covered in the University Student Conduct Code.

### **Instructor and Teaching Assistants**

Dr. P. Thomas Vernier is the course instructor. Telephone 310.448.8752. E-mail [Vernier@usc.edu](mailto:Vernier@usc.edu). Office hours are Tuesday and Thursday, 11:00–12:00 (other times by appointment).

Teaching assistants are Brent Nash ([BNash@usc.edu](mailto:BNash@usc.edu)) and Keith Takishita ([Takishit@usc.edu](mailto:Takishit@usc.edu)).

The course web site is <http://www-classes.usc.edu/engr/ee-ep/327/>.

### **Textbooks**

*Analysis and Design of Digital Integrated Circuits*, Third Edition, David A. Hodges, Horace G. Jackson, and Resve A. Saleh, McGraw-Hill, 2004.

*Physical Design of CMOS Integrated Circuits Using L-Edit*, John P. Uyemura, Brooks/Cole, 1995. (Optional)

### **Other References**

*CMOS Digital Integrated Circuits Analysis and Design*, Third Edition, Sung-Mo (Steve) Kang and Yusuf Leblebici, McGraw-Hill, 2002.

*Digital Integrated Circuits*, Second Edition, Jan M. Rabaey, Anantha P. Chandrakasan, and Borivoje Nikolic, Prentice-Hall, 2002.

*Principles of CMOS VLSI Design*, Second Edition, Neil H. E. Weste and Kamran Eshraghian, Addison Wesley, 1993.

*Principles of CMOS VLSI Design*, Third Edition, Neil H. E. Weste and David Harris, Addison Wesley, 2004.

*Analog Integrated Circuit Design*, David A. Johns and Ken Martin, Wiley, 1997.

*CMOS Mixed-Signal Circuit Design*, R. Jacob Baker, Wiley, 2002.

*Inside SPICE*, Ron Kielkowski, McGraw-Hill, 1994.

*MOSFET Modeling with SPICE*, Daniel Foty, Prentice Hall, 1997.

*Operation and Modeling of the MOS Transistor*, Yannis P. Tsividis, McGraw-Hill, 1987.

*SPICE*, Gordon W. Roberts and Adel S. Sedra, Oxford University, 1997.

*CMOS Circuit Design, Layout, and Simulation*, R. Jacob Baker, Harry W. Li, and David E. Boyce, Wiley, 1998.

*CMOS IC Layout*, Dan Clein, Newnes, 2000.

## EE 327x Course Schedule, Spring 2005

Session	Date	Topic	Text
1	Jan 11	CMOS processes	<i>HJS</i> 1
2	Jan 13	MOS devices	<i>HJS</i> 2.1–2.3
3	Jan 18	MOSFET I-V	<i>HJS</i> 2.4
4	Jan 20	MOSFET I-V	<i>HJS</i> 2.5–2.7
5	Jan 25	MOSFET capacitance	<i>HJS</i> 2.8
6	Jan 27	SPICE models	<i>HJS</i> 3.4–3.7
7	Feb 01	Inverters	<i>HJS</i> 4.1–4.5
8	Feb 03	CMOS inverter	<i>HJS</i> 4.5–4.10
9	Feb 08	Process flow; Layout 1	<i>HJS</i> 3.1–3.3
10	Feb 10	Design flow; Layout 2	<i>U</i> 1, 3, 4.6–4.9
	Feb 15	<b>Midterm Exam 1</b>	
11	Feb 17	Combinational logic	<i>HJS</i> 5.1–5.4
12	Feb 22	MUXs, FFs; Power	<i>HJS</i> 5.5–5.10
13	Feb 24	Timing analysis	<i>HJS</i> 6.1–6.4
14	Mar 01	Gate sizing for delay	<i>HJS</i> 6.5
15	Mar 03	Logical effort	<i>HJS</i> 6.6
16	Mar 08	Interconnect	<i>HJS</i> 10.1–10.4; <i>U</i> 3.7
17	Mar 10	Power grid; clock	<i>HJS</i> 11.1–11.3
	Mar 15	<i>Recess</i>	
	Mar 17	<i>Recess</i>	
18	Mar 22	Layout 3 — Gates	<i>U</i> 5.2.4, 5.5, 5.6
19	Mar 24	Layout 4 — VLSI blocks	<i>U</i> 6
	Mar 29	<b>Midterm Exam 2</b>	
20	Mar 31	Project assignment	
21	Apr 05	SRAM; Project	<i>HJS</i> 8
22	Apr 07	DRAM; ROM; Project	<i>HJS</i> 9.1, 9.4–9.6
23	Apr 12	Drawn, fabricated; Project	
24	Apr 14	CMP; Project	
25	Apr 19	GHz clocks; Project	
26	Apr 21	Process skew; Project	
27	Apr 26	Modern models; Project	
28	Apr 28	<b>Project Due</b>	

*HJS* — Hodges, Jackson, Saleh, *Analysis and Design of Integrated Circuits*  
*U* — Uyemura, *Physical Design of CMOS Integrated Circuits Using L-EDIT*

Final Examination: Thursday, May 5, 2:00–4:00 P.M.