

Young H. Cho

Last Updated 02/18/09

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EDUCATION

- 2005-Ph.D. Electrical Engineering
University of California, Los Angeles, Los Angeles, CA
Supervisors: W.H. Mangione-Smith (Chair), G.J. Pottie, L. He, G. Reinman
Thesis: Deep Content Inspection for High Speed Computer Networks
- 2001-M.S. Electrical and Computer Engineering
University of Texas at Austin, Austin, TX
Supervisor: B.L. Evans (Chair)
Thesis Report: Implementation of a 3-D Sonar Beamformer using Quad PPC G4
- 1996-B.A. Computer Science
University of California, Berkeley, CA
Research Supervisors: David Patterson, David Culler

EMPLOYMENT

COMPUTER SCIENTIST – USC – Information Science Institute – September 2008 to Present
The Network Division (Division7)

- Prepare and submit proposals for R&D grants
- Devise and negotiate cooperative contracts with research institutions and companies
- Responsible for leading research team for established government and private contracts
- Write and submit publications to peer reviewed conferences and journals

POSTDOCTORAL RESEARCHER – University of California, Los Angeles – August 2007 to August 2008
Department of Electrical Engineering – Member of Networked & Embedded Systems Laboratory (NESL) and Center for Embedded Networked Sensing (CENS)

- Prepare and submit proposals for R&D grants
- Devise and negotiate cooperative contracts with research institutions and companies
- Responsible for leading research team for established government and private contracts
- Advise Masters and Doctoral Electrical Engineering students in their research
- Mentor and Instruct laboratory Interns
- Write and submit publications to peer reviewed conferences and journals

Key Achievements:

- 2 patents pending
- 2 accepted + 4 submitted + 2 under preparation peer reviewed publications
- DAC 2008 - Design Competition Winner (Lead)

VISITING PROFESSOR – Washington University in St. Louis – Jul 2005 to Jun 2007

Dept. of Computer Sciences and Engineering – Member of Applied Research Laboratories

- Responsible for leading research team for contract with Disruptive Technology Office
- Design high-speed network content parsing, classification, and clustering system
- Qualitative analysis of the pre-existing system and modification for field operation
- Advise Masters and Doctoral Computer Engineering students in their research
- Instruction in Graduate-level Computer Architecture course offered at the university

Key Achievements:

- Successful development of multi-Gbps e-mail content parsing system
- Designed functional prototype of multi-Gbps content based network router, payload classification, and clustering system
- Development of novel architecture to enable optimal FPGA design performance with safe operating temperature
- Over 15 competitive technical conference, journal, and book chapter publications

GRADUATE RESEARCH ASSISTANT – University of California, Los Angeles – Sep 2001 to Jun 2005
Dept. of Elec Engineering – Compiler and Architecture Research for Embedded Systems

- Research and development in high-performance Network Intrusion Detection Systems
- Design novel architectures for scalable high-speed pattern matchers
- Instruction and Assistance in Upper-division Computer/Electrical Engineering courses

Key Achievements:

- Successful development of multi-Gbps pattern matcher using FPGA and ASIC
- Designed a novel high-performance processor for context free grammar parsing
- 7 competitive technical conference and journal publications
- 1 licensed International patent of pattern matching technology
- 2 patent pending for novel network intrusion detection system technologies

COMPUTER CONSULTANT – U.B. Video, Vancouver, B.C. – Apr 2000 to Aug 2000

Video Compression and Streaming Technology Company

- Research and development of image compression API for image foveation algorithms

Key Achievements:

- Demonstration of image tracking and fast foveation algorithm on real-time video streams

GRADUATE RESEARCH ASSISTANT – University of Texas, Austin – Aug 1999 to Dec 2000

Department of Electrical and Computer Engineering – Applied Research Laboratories

- Research in 3-D Sonar Beamforming Algorithm (AltiVec and Sun VIS)
- Evaluate hardware and software research platforms (Quad PowerPC G4)

Key Achievements:

- Demonstration of accelerated beamforming algorithm using PowerPC AltiVec extensions
- Thorough analysis of the performance bottlenecks and defined platform recommendations
- 2 competitive technical conference publications

RESEARCH ENGINEER/PROGRAMMER – Myricom, Inc. – Jul 1996 to Aug 1999

High Performance Computer Network Company – Creator of Myrinet

- Research and development in distributed FPGA based two-level multi-computer
- Development of high-speed Myrinet networking appliances
- Development of high-performance network testing appliances

Key Achievements:

- Developed several Myrinet commercial products such as Myrinet to Fiber optics converter, Oct Switch, and SAN to LAN converter
- Developed a number of Myrinet test equipments including LANai processor functional test system and FI device tester
- Developed a number of board layout and logic synthesis CAD tools
- Implemented high-performance Automatic Target Recognition system using FPGA based Myricom two-level multicomputers
- 1 competitive technical conference publication

RESEARCH ASSISTANT – University of California, Berkeley – January 1994 to June 1996

Department of Electrical Engineering and Computer Science

- Research in Networks of Workstation (NOW) under David Patterson and David Culler
- Software and Hardware design and support

Key Achievements:

- Designed and built HP/Myrinet Interface
- Embedded system test software

TEACHING EXPERIENCE

Courses Taught

Washington University in St. Louis

- CSE 560M – Graduate Computer Architecture I

UCLA

- CS M152B – Computer Architecture Laboratory (Prof. D. Rennels)
- EE 116B – VLSI Course (Prof. M. Srivastava)
- EE 115C – Digital Electronic Circuits (Prof. B. Daneshrad)

UC Berkeley

- CS 152 – Computer Architecture (Prof. D. Culler)
- CS 152 – Computer Architecture (Prof. D. Patterson)
- Computer Architecture Seminal for Re-entry Students

PhD Student Advising/Mentoring

Ph.D. Graduates:

Phillip Jones (graduated in Jan 2008: Tenure Track Assistant Professor at Iowa State University)
James Moscola (Co-chair in his Ph.D. Committee - graduated in April 2008)

Current UCLA PhD Students:

Zainul Charbiwala, Jonathan Friedman, Thomas Schmid, Roy Shea

Current USC MS Students:

Jui-Hung Chang

HONORS

Design Automation Conference Student Design Competition Winner (Faculty) – 2008
The Best Paper Award – IEEE VLSI Design 2007
John Deere Scholarship, UCLA – 2003
UCLA EE Departmental Fellowship, UCLA - 2002
Altera University Scholarship, UT Austin – 1999
Award of Recognition in Excellency as Teaching Assistant, UC Berkeley – 1996

PROFESSIONAL ACTIVITIES

Refereed Conference Service

- IEEE Globecom Session Chair – 2005

Refereed Conference Paper Reviewer

- IEEE Transactions on Computers, IEEE Transactions on VLSI, IEEE Journal on Selected Areas of Communications, International Journal of Security and Networks, IEEE Transactions on Dependable and Secure Computing, ACM Transactions on Embedded Computing Systems, IEEE/ACM International Symp. On Microarchitecture (MICRO), ACM FPGA, EURASIP JES, IEEE Field Programmable Logic, IEEE International Symposium on Circuits and Systems

Membership

- IEEE (EE) and ACM since 1999

COLLABORATORS AND OTHER AFFILIATIONS

A. Collaborators and Co-authors

Prof. Deborah Estrin (UCLA), Prof. Mani Srivastava (UCLA), Prof. Jeremy Buhler (WashU), Prof. Roger D. Chamberlain (WashU), Prof. Ron Cytron (WashU), Prof. Andre Dehon (U. Pennsylvania), Prof. Scott Hauck (U. Washington), Prof. John W. Lockwood (WashU/Stanford), Prof. William Mangione-Smith (UCLA/Intellectual Ventures), Danny Cohen (Caltech/Myricom/Sun), Dr. Ruth Sivilotti (Myricom), Dr. Wen-King Su (Myricom), Dr. Doyle Weishar (i_SW Corp), Dr. John Byrns (Fair Issac), Dr. Alan Ratner (National Security Agency), John Wroclawski (ISI), Dr. John Heidemann (ISI), Dr. Terry Benzel (ISI)

B. Research Advisors

Primary PhD Thesis Advisor: Prof. William Mangione-Smith (EE, UCLA)

Other PhD Thesis Committee: Prof. Greg Pottie (EE, UCLA), Prof. Lei He (EE, UCLA), Prof. Glenn Reinman (CS, UCLA)

Primary MS Thesis Advisor: Prof. Brian Evans (ECE, UT Austin)

Other Research Advisors: Prof. David Culler (EECS, UC Berkeley), Prof. David Patterson (EECS, UC Berkeley), Dr. Charles Seitz (Caltech/Myricom), Dr. Danny Cohen (Caltech/Myricom/Sun)

C. Post-graduate Mentors/Sponsors

Prof. Mani Srivastava (UCLA), Prof. Deborah Estrin (UCLA), Prof. John W. Lockwood (WashU)

GRANTS

- Current: Satellite Sensornet Gateway – NASA Advanced Information Systems Technology Program – October 2006 to September 2009, Amount: \$1,489,891 – USC – PIs: Terry Benzel and Young H. Cho.
- Current: CISOFIT Steamflooding – Chevron – January 2009 to December 2009, Amount: \$100,000 – USC – PIs: Young H. Cho and John Heidemann.
- Current: CISOFIT Underwater – Chevron – January 2008 to December 2009, Amount: \$200,000 – USC – PIs: John Heidemann and Young H. Cho.
- Past: Fast Semantic Content Processing – Air Force/NSA/Science Applications International Corporations (SAIC) - April 2006 to December 2006, Amount: \$334,092 – Washington University in St. Louis – PIs: John W. Lockwood, Young H. Cho and Ron Loui.
- Submitted: Software acoustic modems for adaptive underwater communication on an open platform – USC/UCLA/Northeastern U. – NSF NeTS – PIs: John Heidemann, Young H. Cho, Mani Srivastava, Milica Stojanovic.
- Submitted: Green Edge Networks – USC/UCLA – NSF CISE Cross Cutting – PIs: Ramesh Govindan, Young H. Cho, Mani Srivastava, and William Kaiser.
- In process: Distributed Reconfigurable Wide-band RF Sensing Platform for Cognitive Radio in Campus-wide WiFi Network Environment – UCLA/USC – NSF GPO Second GENI Solicitation – PIs: Young H. Cho and Danijela Cabric.
- In process: Inspecting Networked Embedded Systems – UCLA/USC – NSF Cyber Physical Systems – PIs: Mani B. Srivastava, Todd Millsetin, Ramesh Govindan, and Young H. Cho.
- In process: Self Sustaining Adaptive Wireless Sensors – USC – NSF Cyber Physical Systems – PI: Young H. Cho.
- In process: Underwater Communication using Electrostatic Field – UCLA/USC – DARPA Seedling Funding - PIs: Young H. Cho and Mani Srivastava.

PATENTS

1. "Oscillator based Drift Compensation Resonator and Timer," UCLA Case No. 2008-769, Inventors: Young H. Cho, Zainul M. Charbiwala, Thomas Schmid, Jonathan Friedman, Mani B. Srivastava; Applicant: University of California, Submission Date: May 23, 2008.
2. "Highly Stable Software Compensated Oscillator," UCLA Case No. 2008-356, Inventors: Young H. Cho, Thomas Schmid, Zainul M. Charbiwala, Mani B. Srivastava; Applicant: University of California, Submission Date: November 23, 2007.
3. "High-Performance Context-Free Parser for Polymorphic Malware Detection," International Patent No: WO2006113722; Inventors: Young H. Cho and William Mangione-Smith; Applicant: University of California, Publication Date: October 26, 2006.
4. "Method And Apparatus For Deep Packet Inspection," International Patent No: WO2006031496; Inventors: Young H. Cho and William Mangione-Smith; Applicant: University of California, Publication Date: March 23, 2006.
5. "Programmable Hardware for Deep Packet Filtering," International Patent No: WO2005104443, EP173853; Inventors: Young H. Cho and William Mangione-Smith; Applicant: University of California, Publication Date: November 3, 2005.

PUBLICATIONS

Book Chapter

- B1. Young H. Cho, "Automatic Target Recognition Application using Field Programmable Gate Array," as part of Reconfigurable Computing: The Theory and Practice of FPGA-Based Computation by Scott Hauck and Andre Dehon, Morgan Kaufmann, Nov. 2007.

Papers Submitted for Review and Papers in Preparation

- R1. Jui-Hung Chang and Young H. Cho, "Impact of Intelligence to Long Term Remote Environmental Monitoring Sensor Systems," in preparation for IPSN Workshop on Sensor Networks for Earth and Space Science Applications ESSA 2009.
- R2. James Moscola, Ron K. Cytron, and Young H. Cho, "Hardware-Accelerated RNA Secondary-Structure Alignment." Submitted to ACM Transactions on Reconfigurable Technology and Systems, December 2008.

Refereed Journal Publications

- J1. Young H. Cho and William H. Mangione-Smith, "Deep Network Packet Filter Design for Reconfigurable Devices." ACM Transactions on Embedded Computing Systems (ACM TECS), 2007.
- J2. James. Moscola, Young H. Cho, and John W. Lockwood, "High Performance Grammar Parsing Hardware for Network Packet Payload Processing." Special issue of ACM Transaction on Design Automation of Electronic Systems on "Demonstrable Software Systems and Hardware Platforms" (ACM TODAES), 2007.

Refereed Conference Publications

- C1. Jonathan Friedman, Thomas Schmid, Zainul Charbiwala, Mani B. Srivastava, Young H. Cho, "Multistatic Pulse-Wave Angle-of-Arrival-Assisted Relative Interferometric Radar," to be presented at IEEE Radar Conference 2009, Pasadena, May 2009.
- C2. Thomas Schmid, Jonathan Friedman, Zainul M Charbiwala, Young H Cho, Mani B Srivastava, "The True Cost of Accurate Time," USENIX Workshop on Power Aware Computing and Systems, December 2008.
- C3. Jonathan Friedman, Zainul M Charbiwala, Thomas Schmid, Young H Cho, Mani B Srivastava, "Angle-of-Arrival Assisted Radio Interferometry (ARI) Target Localization," Proceedings of MILCOM 2008, November 2008.
- C4. Thomas Schmid, Jonathan Friedman, Zainul M Charbiwala, Young H Cho, Mani B Srivastava, "Low-Power High-Accuracy Timing Systems for Efficient Duty Cycling," ISLPED 2008 , August 2008.
- C5. Thomas Schmid, Zainul M Charbiwala, Jonathan Friedman, Young H Cho, Mani B Srivastava, "**Exploiting Manufacturing Variations for Compensating Environment-induced Clock Drift in Time Synchronization,**" ACM Sigmetrics 2008 , June 2008.
- C6. Thomas Schmid, Jonathan Friedman, Zainul M Charbiwala, Young H Cho, Mani B Srivastava, "XCXO: An Ultra-low Cost Ultra-high Accuracy Clock System for Wireless Sensor Networks in Harsh Remote Outdoor Environments," ISSCC/DAC 2008, (Unpublished Student Design Contest Entry, Award Winner) , February 2008.
- C7. Phillip H. Jones, James Moscola, Young H. Cho, and John W. Lockwood, "**Adaptive Thermoregulation for Applications on Reconfigurable Devices.**" 17th IEEE International Conference on Field Programmable Logic and Applications (FPL), Amsterdam, Netherlands, August 27-29, 2007. [~21% acceptance rate]
- C8. Moshe Looks, Ronald P. Loui, John W. Lockwood, Adam Covington, Andrew Levine, Young H. Cho, "Streaming Hierarchical Clustering for Text Mining." IEEE Aerospace Conference, Big Sky, MT, March 3-10, 2007.
- C9. Andrew Levine, Ronald P. Loui, John W. Lockwood, Young H. Cho, "Sensitivity Analysis of Gigabit Concept Mining System." IEEE Aerospace Conference, Big Sky, MT, March 3-10, 2007.
- C10. James Moscola, Young H. Cho, and John W. Lockwood, "Hardware-Accelerated Parser for Extraction of Metadata In Semantic Network Content." IEEE Aerospace Conference, Big Sky, MT, March 3-10, 2007.
- C11. Phillip H. Jones, Young H. Cho, and John W. Lockwood, "**Dynamically Optimizing FPGA Applications by Monitoring Temperature and Workloads.**" 20th IEEE/ACM International Conference on VLSI Design, Bangalore, India, January 6-10, 2007. [**Best Paper of VLSI Design Conference**]
- C12. Phillip H. Jones, Young H. Cho, and John W. Lockwood, "An Adaptive Frequency Control Method using Thermal Feedback for Reconfigurable Hardware Applications." IEEE

- International Conference on Field Programmable Technology (FPT), Bangkok, Thailand, December 13-15, 2006.
- C13. James M. Moscola, Young H. Cho, and John W. Lockwood, "A Reconfigurable Architecture for Multi-gigabit-Speed Content-based Routing." 14th IEEE Hot Interconnects, Stanford, CA August 23-25, 2006.
 - C14. G. Adam Covington, Charles L.G. Comstock, Andrew A. Levine, John W. Lockwood, Young H. Cho, "High Speed Document Clustering in Reconfigurable Hardware." 16th IEEE International Conference on Field Programmable Logic and Applications (FPL), Madrid, Spain, August 2006. (~27% acceptance rate)
 - C15. Phillip H. Jones, John W. Lockwood, and Young H. Cho, "A Thermal Management and Profiling Method for Reconfigurable Hardware Applications." 16th IEEE International Conference on Field Programmable Logic and Applications (FPL), Madrid, Spain, August 2006. (~27% acceptance rate)
 - C16. Young H. Cho, James M. Moscola, and John W. Lockwood, "**Context-Free Grammar based Token Tagger in Reconfigurable Devices.**" IEEE ICDE - International Workshop on Semantics enabled Networks and Services (ICDE SeNS), April 3-7, Atlanta, GA, 2006.
 - C17. Young H. Cho and William H. Mangione-Smith, "High Performance Context Free Grammar Parser for Network Intrusion Detection." Advanced Networking and Communications Hardware Workshop (ANCHOR), Madison, Wisc, Wisconsin, June 2005.
 - C18. Young H. Cho and William H. Mangione-Smith, "**A Pattern Matching Co-processor for Network Security.**" 42nd IEEE/ACM Design Automation Conference, Anaheim, CA, June 13-17, 2005. [~20% acceptance rate]
 - C19. Young H. Cho and William H. Mangione-Smith, "Fast reconfiguring Deep Packet Filter for 1+ Gigabit Network." IEEE Symposium on Field-Programmable Custom Computing Machines (FCCM), Napa Valley, CA, April 2005. (~28% acceptance rate)
 - C20. Young H. Cho and William H. Mangione-Smith, "Programmable Hardware for Deep Packet Filtering on a Large Signature Set." First Watson Conference on Interaction between Architecture, Circuits, and Compilers(P=ac2), Yorktown, NY, Oct. 6-8, 2004
 - C21. Young H. Cho and William H. Mangione-Smith, "Deep Packet Filter with Dedicated Logic and Read-Only-Memories." IEEE Symposium on Field-Programmable Custom Computing Machines (FCCM), Napa Valley, CA, April 2004. (~27% acceptance rate)
 - C22. Young H. Cho and William H. Mangione-Smith, "Specialized Hardware for Deep Network Packet Filtering." International Conference on Field Programmable Logic and Applications (FPL), Montpellier, France, Sep. 2002.
 - C23. Young H. Cho, David Brunke, Greg Allen, and Brian Evans, "Optimization of Vertical and Horizontal Beamforming Kernels on the PowerPC G4 Processor with AltiVec Technology." 34th IEEE Asilomar Conference on Signals, Systems, and Computers, Monterey, CA, October 2000.
 - C24. Young H. Cho, "Optimized Automatic Target Recognition Algorithm on Scalable Myrinet/Field Programmable Array Nodes." 34th IEEE Asilomar Conference on Signals, Systems, and Computers, Monterey, CA, October 2000.
 - C25. Ruth Sivilotti, Young H. Cho, Wen-King Su, Danny Cohen, and Brian Bray, "Scalable Network Based FPGA Accelerators for an Automatic Target Recognition Application." IEEE Symposium on Field-Programmable Custom Computing Machines (FCCM), Napa Valley, CA, April 1998.

Refereed Posters

- O1. Thomas Schmid, Jonathan Friedman, Zainul M Charbiwala, Young H Cho, Mani B Srivastava, "XCT: Crystal Compensated Timer for Low-cost, Low-drift Clocks," ISSCC 2008 , February 2008.
- O2. Phillip H. Jones, James Moscola, Young H. Cho, and John W. Lockwood, "Changing Output Quality for Thermal Management." IEEE Symposium on Field-Programmable Custom Computing Machines (FCCM), Napa Valley, CA, April 2007.

- O3. James Moscola, Young H. Cho, and John W. Lockwood, "Implementation of Network Application Layer Parser for Multiple TCP/IP Flows in Reconfigurable Devices." IEEE 16th International Conference on Field Programmable Logic and Applications (FPL), Madrid, Spain, August 2006.
- O4. James Moscola, Young H. Cho, and John W. Lockwood, "Content-Free Grammar Parsing for High-Speed Network Applications in Reconfigurable Hardware." 9th SIGDA Ph.D. Forum at DAC 2006, San Francisco, CA, July 25, 2006.
- O5. James M. Moscola, Young H. Cho, and John W. Lockwood, "A Scalable Hybrid Regular Expression Pattern Matcher." IEEE Symposium on Field-Programmable Custom Computing Machines (FCCM), Napa Valley, CA, April 2006.
- O6. Arpith C. Jacob, Brandon Harris, Jeremy Buhler, Roger Chamberlain, and Young H. Cho, "Scalable Softcore Vector Processor for Biosequence Applications." IEEE Symposium on Field-Programmable Custom Computing Machines (FCCM), Napa Valley, CA, April 2006.
- O7. Shobana Padmanabhan, Moshe Looks, Dan Legorreta, Young Cho, and John W. Lockwood, "A Hardware Implementation of Hierarchical Clustering." IEEE Symposium on Field-Programmable Custom Computing Machines (FCCM), Napa Valley, CA, April 2006.
- O8. James M. Moscola, Young H. Cho, and John W. Lockwood, "Reconfigurable Context-Free Grammar based Data Processing Hardware with Error Recovery." 13th IEEE Reconfigurable Architectures Workshop (RAW), Rhodes Island, Greece, April 2006.
- O9. Young H. Cho, James M. Moscola, and John W. Lockwood, "Context-Free Grammar based Token Tagger in Reconfigurable Devices." 14th ACM/SIGDA International Symposium on Field-Programmable Gate Array (FPGA), Monterey, CA, February 2006.

Non-Refereed Publications

- N1. Wen-King Su, Young H. Cho, Ruth Sivilotti, and Danny Cohen "Scalable, Network-Connected, Reconfigurable, Hardware Accelerators for an Automatic-Target-Recognition Application." Tech Report, Defense Advanced Research Projects Agency, May 1998.
- N2. Wen-King Su, Young H. Cho, Ruth Sivilotti, Danny Cohen, and Brian K. Bray, "Myricom's FPGA based Approach to ATR/SLD." ARPA/ACS-PI-Meeting Presentation, November 1997.
- N3. Phillip H. Jones, Young H. Cho, and John W. Lockwood, "Adaptive Control of FPGA Computation with Thermal Feedback." The Syndicated, Q4, 2006.

REFERENCE

References available upon request