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MOSIS: Present and Future

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MOSIS is DARPA's MOS Implementation System. For the past three years it has provided packaged parts for over 2,000 VLSI design projects submitted by designers from over 60 organizations. Currently, MOSIS provides 1,300 projects a year in nMOS, CMOS/Bulk and CMOS/SOS technologies and also provides access to PCB fabrication. This paper discusses the services MOSIS currently offers and those that it is preparing to offer.

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Invited Talk
MOSIS: PRESENT AND FUTURE

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INTRODUCTION

MOSIS is DARPA's MOS Implementation System. For the past three years it has provided packaged parts for over 2,000 VLSI design projects submitted by designers from over 60 organizations. Currently, MOSIS provides 1,300 projects a year in nMOS, CMOS/Bulk, and CMOS/SOS technologies and also provides access to PCB fabrication.

MOSIS is not involved in the actual fabrication of parts or boards. Its main function is to act as a single interface between a geographically distributed design community and a diverse semiconductor industry. As such an interface, MOSIS has significantly reduced the cost and time associated with prototyping custom chips and custom boards. This in turn has opened up VLSI technology to a much broader segment of the systems design community.

This paper discusses the services MOSIS currently offers and those that it is preparing to offer.

GEOMETRY TO PROTOTYPE PACKAGED PARTS

Technologies

Designers encode the geometrical information that they want instantiated on silicon in text files and transmit them to MOSIS either over the ARPANET, CSNET, MILNET (or any other network communicating with the ARPANET), or via TELEMAIL. The format in which this geometrical information is encoded is known as the Caltech Intermediate Form, or CIF (Ref. 1). In four to thirteen weeks, depending on the technology, they receive packaged parts with a diagram showing which pad is connected to which pin of a package. Information regarding SPICE and other parameters extracted from test structures on their run is available to them through electronic mail.

Designers can submit projects in any one of the following technologies: 4 and 3 micron nMOS, 3 micron CMOS/Bulk, 4 micron CMOS/SOS. One set of design rules and CIF layer conventions are associated with each technology. These design rules have been assembled under the constraint that they be acceptable by a reasonable vendor base to which MOSIS interfaces.

MOSIS's nMOS fabrication is based on the well known Mead-Conway lambda rules (Ref. 1) which scale with a single parameter lambda. Feature sizes of 3 and 4 microns are currently supported. Therefore, nMOS designers can scale their circuitry (with the exception of pads) from one feature size to another. However, because of the paucity of fabricators capable of supporting 3 micron rules, the majority of nMOS runs are at 4 microns. They are held every three weeks, and 3 micron runs are held approximately four times a year.

MOSIS has experienced that nMOS wafer fabrication turnaround ranges from one to three weeks.

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There is no effort to develop a larger vendor base for finer feature nMOS because of expected power density limitations.

CMOS/Bulk is the emerging technology. MOSIS has adopted the philosophy that 3 micron CMOS/Bulk is going to be the work horse of the design community for the next ten years. Only in special cases will designers opt for a finer feature size, expected to be 1.2 microns.

MOSIS plans to rapidly expand its vendor base for 3 micron CMOS/Bulk based upon a set of design rules already in hand. Currently, five fabricators provide turnaround ranging from four to thirteen weeks.

MOSIS is taking steps to position its design community to exploit the 1.2 micron CMOS/Bulk technology that is being developed at several United States industrial laboratories. Towards this goal, MOSIS is supporting a number of investigators in their development of rules and design techniques for 1.2 micron CMOS/Bulk, with wafer fabrication carried out by four vendors. The idea is to develop these rules and techniques in parallel with the development of the technology--thus allowing the entire MOSIS community to use this technology upon the completion of its development. This strategy will narrow the gap inherent in waiting for a new technology to become available before learning how to use it.

An interesting note on the 1.2 micron CMOS/Bulk activity is that measurements on wafers are being carried out by MOSIS according to test code supplied by various experimenters. Test results (as opposed to dies or wafers) are then distributed to the experimenters. This course is being taken to avoid casual perusal of the fabricators' technology, which they consider very sensitive and proprietary at this stage.

Testing and Packaging

Most of the designers in the MOSIS community are designing small prototype circuits which they intend to incorporate into larger circuits. They typically require a small number of parts; most are satisfied with one to three parts as long as the probability of getting defectless parts is high. To accommodate these designers, MOSIS holds multiproject runs as first described in Ref 1. Electron beam technology is used to make master 1X plates containing as many as 50 different die types, each containing several different projects. Therefore, the cost of a run to a designer, if it were to be borne by him, could be made proportional to the fraction of the area his design(s) occupied on the wafer. This cost would be only a small fraction of the total cost of the run. Sharing silicon makes the proposition of incremental development and debugging of designs economically viable (Fig. 1).

Wafer acceptance is based on measurements by vendors and by MOSIS on commonly agreed-upon test structures on wafers, as opposed to functional performance of any design. These are simple structures such as inverters, individual transistors, structures to measure sheet and contact resistances, and capacitors. They are easily contained in a test strip which is incorporated into every die type in a run. MOSIS has an automated parametric tester which allows the measurement of every test strip on every die on every wafer of a run. These measurements form the basis of acceptance of wafers and then the selection of those to be separated and assembled into parts.

MOSIS's current packaging strategy is to package enough parts for a designer so as ensure him 90% probability of receiving a defectless part. Screening to prevent packaging of defective parts is not done yet. This strategy was acceptable when most of MOSIS's community was designing small circuits and the fraction of packaged defective parts was small.

A significant portion of the community has successfully completed the development of large designs and now wants from 300 to 3,000 working parts to begin developing prototype systems based on parts obtained through MOSIS. The yield for these large designs is expected to be 25% at best. If MOSIS were to follow its current strategy of packaging parts without any testing to indicate functionality, it would be packaging four times as many parts to achieve a requested quantity. This becomes a serious problem as quantities increase. Packaging costs dictate a more economical approach.

To avoid such waste, MOSIS has worked with Stanford University to define a functional test language (SIEVE) and is developing hardware to effect the testing specified by that language. Users will soon have the option to submit text describing limited test procedures to be used at wafer probe to screen out bad parts. The purpose of this screening is to detect the types of "trival" defects that cause the majority of bad parts and, therefore, to reduce packaging costs. Full functional testing is expected to be done by the user.

For designs with custom pad layouts it will be the responsibility of the designer to provide MOSIS with the custom probe card to probe his circuits. To eliminate the inconveniences associated with generating custom probe cards for every design, MOSIS is currently developing a set of standard pad frames each specifying exactly where the pads are posititioned. MOSIS will then stock probe cards for each of the frames.

These standard frames are also expected to facilitate packaging. Bonding diagrams for projects currently submitted are generated manually, because several attempts to automate this process have been less than perfect. Bonding diagrams instruct the packager to connect a specific pad on the chip to a specific pin on the package. With standard pad frames (and, therefore, standard bonding diagrams), the need to generate new diagrams for each project will be eliminated.

Standard frames also allow the bonding process itself to be automated. Automated, programmable bonding machines are currently available. Standard pad frames make possible a scenario where an operator would identify a first pad and package pin; programmed information would then control the bonding on a chip.

Automating the packaging phase could significantly improve MOSIS's turnaround time. The best times experienced by MOSIS for various parts of a run in nMOS are (1) four days to convert submitted geometry into a format acceptable by a mask maker and to generate the first masks required by a fabricator to start a run, (2) five days for wafer fabrication, (3) one day for wafer acceptance, (4) one week for packaging, and (5) one day for overnight delivery of packages. Standard pad frames with automated bonding could reduce packaging time to two or three days and reduce the time from submission of designs to mailing of packaged parts (in very conventional technologies) to approximately two weeks.

PRINTED CIRCUIT BOARDS

A recently added service offered by MOSIS is the fabrication of Printed Circuit Boards (PCBs). MOSIS treats PCBs as just another technology, surprisingly similar to nMOS and the various dialects of CMOS.

PCBs, like integrated circuits, are fabricated by a process that produces a series of two-dimensional images of possibly different properties, constructed on top of each other. The conducting and insulating layers communicate with each other through vias with patterns for that purpose, and also have electrical interaction where certain spatial relations hold, e.g., transistors and inter-layer impedance.

Although PCBs and ICs are made of different materials, they share a common method of specification of the images required on each of their layers. Both are fabricated by a

"photographic" process which transfers images to the media surface from a master tooling.

The single most important difference between these technologies is the scale, or "feature size". A typical IC device has a feature size of 3 microns and a size of 6mm; hence it is 1,000 line-pairs across. A typical PCB has a feature size of 0.004 inches and a size of 16 inches; hence 2,000 line-pairs. These numbers show that the resolution of the tooling is not significantly different between these two technologies. The most significant difference, as far as fabrication preparation (the job of MOSIS) is concerned, is the size. Both technologies use 1X tooling.

Realizing these similarities and differences, the MOSIS user community decided to extend their VLSI design and fabrication tools to accommodate PCBs as well. The simple first steps already taken treat PCBs as yet another technology, with its own set of conventions, standard cells and, obviously, its own geometric and electric design rules. As with IC designs, the PCB patterns are expressed in CIF; from the viewpoint of the user, MOSIS treats the geometric processing required to convert CIF into tooling for PCBs just as it does any other technology.

These technologies differ significantly in fabrication philosophy. The unit of production in the IC arena is a wafer which may have many different die-types, each possibly with several independent projects. PCBs, on the other hand, are rarely combined in the fabrication process. Therefore, MOSIS does not apply its standard Multi-Chip-Project and Multi-Chip-Wafers procedures to PCBs, but fabricates them one at a time.

Conventional tooling for ICs is a set of 1X masks, typically 5 inches square. The conventional tooling for PCBs is a set of 1X films, typically 20 inches square. The former are usually made by E-beam machines, the latter by photo-plotters (and soon also by lasers).

Neither E-beam machines nor photo-plotters can use the CIF format directly. These families of equipment require data formats of totally different natures: E-beam machines are most efficient while traversing a predefined scan, whereas the electro-mechanical photo-plotters enjoy the ability to use random motion. All the upcoming laser writers are expected to be similar to the E-beam pattern generators rather than to the conventional electro-mechanical photo-plotters.

Due to the limitation of the old photo-mechanical equipment used for photo-plotters, all of the data formats ("languages") suffer from various archaic idiosyncracies, guaranteed to rule out any compatibility among the various vendors.

Complying with these idiosyncracies and passing them to the designers (in form of design rules, for example) is diametrically opposed to the MOSIS philosophy. It was therefore decided to stay with the same "combat proven" IC tooling preparation method for PCBs. Hence, MOSIS generates the patterns for all PCB layers by using E-beam technology, which produces high-quality glass plates instead of larger patterns on sheets of film.

Economy, the availability of software for E-beam machines, and the ratio of feature size between IC and PCB technologies, suggested that the glass plates be made at 0.05X. This scale allows the generation of 16 patterns, each of 20"x20" target size, on a standard 5"x5" plate. A simple (and inexpensive) photographic process is used to transfer these images from the glass plates to film sheets. The required magnification of 20X is an integral part of this photographic process. The resolution of the photographic process has to support only 2,000 line-pairs across the whole image, well under the limitation of good lenses.

This approach of using common tooling preparation methodology for both ICs and PCBs has many advantages; it allows designers to use common tools for the design process (with details tailored specifically to

each technology) and allows MOSIS to apply the same management procedures and the same geometrical processing and tooling preparation methods to PCB technology.

An important unexpected benefit of this approach is the existence of the master tooling on high-quality glass, which does not flex, stretch, scratch or deteriorate with time. It is easy and common to protect glass mask masters from environmental hazards.

Probably the most important feature of the expansion of MOSIS to include PCBs is that the expansion has been done in a way which is expected to carry over to other packaging technologies, such as various hybrids, ceramic carriers, and plastic tapes.

MOSIS has already published design rules, recommended procedures, and various standard cells and design frames for PCBs, and the service is being used.

By adhering to the notion of separation of design from fabrication, MOSIS refused to burden its users with many of the traditional idiosyncracies involved in PCB design, especially those arising from aperture-related constraints. Although unconventional, the route to PCB tooling through 0.05X E-beam masks has proven to be not only versatile, but economical.

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[1] Mead, C.A., and Conway, Lynn, *Introduction to VLSI Systems*, Addison-Wesley, 1981.