Andrew G. Schmidt

Computer Scientist
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Education

Ph.D. Electrical Engineering, University of North Carolina at Charlotte
Dissertation Topic: *Productively Scaling Hardware Designs over Increasing Resources Using a Systematic Design Analysis Approach*
Major Advisor: Dr. Ron Sass
M.S. Computer Engineering, University of Kansas
B.S. Computer Engineering, University of Kansas

Research Objectives

I am broadly interested in reconfigurable computing, computer architecture, high performance computing (HPC), and embedded systems. My current research is investigating efficient utilization of heterogeneous resources through static analysis and runtime performance monitoring. I am immediately interested in extending this research to explore a more diverse set of heterogeneous resources, as well as, the applicability of such monitoring approaches to make high performance embedded computing (HPEC) more resilient.

Employment

Computer Scientist — Matthew French
Information Sciences Institute — July 2011 – Current

As a Computer Scientist in the Reconfigurable Computing Group at USC's Information Sciences Institute I apply my expertise in reconfigurable computing and FPGAs, computer architecture, high performance computing (HPC), and embedded systems with focuses on hardware heterogeneity and Trust. Current research includes hardware/software co-design programming models and their integration with network-on-chips and multiple processor systems, resilient high performance reconfigurable computing tools and techniques, a sophisticated hardware performance monitoring infrastructure for runtime analysis of system-on-chip designs, and efficient utilization of heterogeneous resources through static analysis and runtime monitoring. This work has directly contributed to numerous DARPA, IARPA, NSF, NASA, and other funded research projects. I am the lead developer of Redsharc, the REconfigurable Data-Stream Hardware Software ARChitecture (Redsharc), which is a programming model and network-on-a-chip solution designed to scale to meet the performance needs of multi-core systems on a programmable chip.

Graduate Research Assistant — Dr. Ron Sass
UNC Charlotte — Summer 2007 – July 2011

As a GRA I lead the development and implementation of the Reconfigurable Computing Cluster project under the management of Dr. Ron Sass. The research included the investigation of using FPGAs for High Performance Computing. We built a small-scale 64 all-FPGA node cluster to evaluate several performance criteria: network performance, memory bandwidth, power consumption, programmability, and system software. As a research assistant, my involvement has been at every level, from assembly of the 64 node cluster, to the creation of custom key IP hardware cores for memory and network infrastructure.

Software Engineer Intern Hugh Khan
Perceptive Software, Inc. June 2005 – January 2007
The internship included the migration of four existing installation applications for the company's software from an older, no longer supported, installation manager to InstallShield. The migration included a complete revision in the installation process, as well as maintenance for existing installations. After the success of the migration, I created and maintained eight additional installers for specific applications that were part of the ImageNow software suite.

Software Development Intern David Duello
Cerner Corporation Summer 2004
As an intern in the product imaging department, I assisted with the development of an imaging database application for MRI images. Part of the development included the implementation of a temporal locality caching system for the imaging database. The application was initially conceived as a standalone application (prototyped with Visual Basic); however, towards the end of my internship I was assigned to restructure the imaging application as a web applet using Java, JavaScript, and HTML.

Research Experience

Reconfigurable Computing Cluster Project
Dr. Ron Sass UNC Charlotte
Summer 2005 – July 2011
The RCC project investigates the use of FPGAs for High Performance Computing. A small-scale 64 all-FPGA node cluster was assembled to evaluate the scalability of the FPGA cluster. The research is centered around several performance assessments, including network performance, memory bandwidth, power consumption, programmability, and system software. As a research assistant, my involvement has been at every level, from assembly of the 64 node cluster, to the creation of custom key IP hardware cores for memory and network infrastructure.

Reconfigurable Data-Stream Software/Hardware Architecture (Redsharc)
Matthew French / Ron Sass Information Sciences Institute / UNC Charlotte
Spring 2009 – July 2011
As a subcontract with the University of Southern California's Information Sciences Institute, UNC Charlotte built Redsharc, a programming model and two network-on-chip solution designed to scale and meet the performance needs of multi-core systems on a programmable chip. Redsharc uses an abstract API that allows programmers to develop systems of simultaneously executing kernels, in software or hardware, that communicate over a seamless interface. My contributions were in the development of two custom network-on-chips, the hardware kernel interface, system software, software API, and several experimental hardware kernels.

Master's Thesis: Quantifying Effective Memory Bandwidth of Platform FPGAs
Advisor: Ron Sass University of Kansas
Fall 2005 – Spring 2007
As part of the Reconfigurable Computing Cluster project, my Master's thesis investigates several common bus architectures common to Platform FPGAs in order to measure the effective bandwidth between High Performance Computing cores and off-chip memory. The results of this research has lead to significant improvements in the on-chip interconnects, memory controllers, and custom memory interfaces used in the RCC project.

Teaching Experience

Visiting Instructor
Dr. Ian Ferguson UNC Charlotte
Fall 2010
Taught one section of the Electrical and Computer Engineering 2181 course, Logic System Design

I, with 40 students. ECE 2181 is a sophomore level course taken by both electrical and computer engineering undergraduates. My responsibilities included creating and presenting lectures, exams, quizzes, homework assignments, and labs. The course covered: binary number systems, Boolean logic and algebra, combinational and sequential circuit design, flip-flops, registers, counters, and other component design, Schematic Capture and logic simulations, hardware description languages, synthesis and testing on a Xilinx Spartan FPGA. Teaching evaluations are available upon request.

Graduate Teaching Assistant
Dr. Nancy Kinnersley — EECS Department, University of Kansas
Fall 2005 – Spring 2007

Taught two sections a semester, for four semesters, of the Electrical Engineering and Computer Science 128 course, Introduction to Computer-Based Information Systems, with approximately 40 students per semester. EECS 128 is offered for undecided engineers or non-engineering majors and is typically taken by sophomores. My responsibilities included creating and presenting lectures, and creating and grading exams, quizzes, and lab assignments. The course covered: computer architecture, system software, application software, binary numbers and Boolean logic, databases, and mobile computing. Teaching evaluations are available upon request.

Awards and Honors

Best Paper Winner – *Merging Programming Models and On-Chip Networks to Meet the Programmable and Performance Needs of Multi-Core Systems on a Programmable Chip.* International Conference on Reconfigurable Computing and FPGAs (ReConFig'10).

OpenFPGA Award Winner – *Investigating Resilient High Performance Reconfigurable Computing with Minimally-Invasive System Monitoring.* International Workshop on High-Performance Reconfigurable Computing Technology and Applications (HPRCTA'10).

Outstanding Graduate Student Award — University of North Carolina at Charlotte

William States Lee Fellowship – University of North Carolina at Charlotte

Graduate Research Assistantship Award — University of North Carolina at Charlotte

Paul F. Huebner Graduate Teaching Assistant Award – University of Kansas

Dale Rummer Senior Design Award – University of Kansas

Skills

FPGAs:

- Xilinx Virtex 2 Pro – UltraScale+ FPGAs
- Altera Stratix III – Stratix10 FPGAs

Tools:

- **Open Source**: Tools for Open Reconfigurable Computing (Torc), RapidSmith
- **Xilinx**: Xilinx Platform Studio (XPS), Integrated Software Environment (ISE), Embedded Development Kit (EDK), Software Development Kit (SDK), ChipScope Pro, PlanAhead, Partial Reconfiguration
- **Altera**: Quartus II
- **Synopsys**: Synplify Premier, Design Compiler, VCS MX Simulator
- **Mentor Graphics**: ModelSim

Linux: Kernel development and custom device driver development

Languages: VHDL, Verilog, C, C++, Java, Python, Scheme, Haskell, Visual Basic

Professional Memberships and Activities

IEEE Computer Society Member: 2004–

ACM Member: 2009–

Order of the Engineer: 2005–

UNC Charlotte Graduate and Professional Student Government Finance Committee: 2010–2011

UNC Charlotte Electrical and Computer Engineering Graduate Association President: 2009–2011

UNC Charlotte 49er and Social Ballroom Dance Club Events Coordinator: 2008–2011

University of Kansas School of Engineering Recent Graduate Advisor Board: 2005–2010

University of Kansas Graduate Engineering Association Treasurer: 2005–2007

University of Kansas Engineering Student Council President: 2004–2005

University of Kansas Student Senate Elections Commission: 2004–2005

University of Kansas Engineering Student Ambassador: 2003–2007

National Association of Engineering Student Councils Central Region President: 2004–2005

Service

High Performance Reconfigurable Computing Track Co-Char, Reconfigurable Computing and FPGAs (ReConFig) 2014–

Program Committee, International Symposium on Field-Programmable Custom Computing Machines (FCCM) 2015–

Program Committee, Reconfigurable Computing and FPGAs (ReConFig) 2011–

Transactions on Reconfigurable Technology and Systems Reviewer: 2012–

Computers Journal Reviewer: 2012–

Publications

Books

[1] Ron Sass and **Andrew G. Schmidt**. *Embedded Systems Design with Platform FPGAs: Principles & Practices*. Morgan-Kaufmann, an imprint of Elsevier, San Francisco, CA, USA, 2010.

Journals

[1] **Andrew G. Schmidt**, Neil Stiner, Matthew French, and Ron Sass. Hwpmi: An extensible performance monitoring infrastructure for improving hardware design and productivity on fpgas. *International Journal of Reconfigurable Computing*, December 2012.

[2] **Andrew G. Schmidt**, William V. Kritikos, Shanyuan Gao, and Ron Sass. An evaluation of an integrated on-chip/off-chip network for high performance reconfigurable computing. *International Journal of Reconfigurable Computing*, April 2012.

[3] **Andrew G. Schmidt**, Siddhartha Datta, Ashwin A. Mendon, and Ron Sass. Investigation into scaling i/o bound streaming applications productively with an all-FPGA cluster. *Parallel Computing*, December 2011.

[4] William V. Kritikos, **Andrew G. Schmidt**, Ron Sass, Erik K. Anderson, and Matthew French. Redsharc: A programming model and on-chip network for multi-core systems on a programmable chip. *International Journal of Reconfigurable Computing*, December 2011.

[5] Ashwin Mendon, **Andrew G. Schmidt**, and Ron Sass. A hardware filesystem implementation with multi-disk support. *International Journal of Reconfigurable Computing*, September 2009.

Symposia and Conferences

[1] Sam Skalicky, Sonia Lopez, Marcin Lukowiak, and **Andrew G. Schmidt**. A parallelizing matlab compiler framework and run time for heterogeneous systems. In *Proceedings of the 17th Annual International Conference on High Performance Computing and Communications (HPCC'15)*. IEEE, 2015.

[2] Sam Skalicky, **Andrew G. Schmidt**, Sonia Lopez, and Matthew French. A unified hardware/software MPSoC system construction and run-time framework. In *Proceedings of the 18th International Conference on Design, Automation and Test in Europe (DATE'15)*. IEEE, 2015.

[3] Sam Skalicky, **Andrew G. Schmidt**, and Matthew French. High level hardware/software embedded system design with redsharc. In *Proceedings of the 1st Annual International Workshop on FPGAs for Software Programmers (FSP'14)*. arXiv.org, 2014.

[4] **Andrew G. Schmidt** and Matthew French. Fast lossless image compression with radiation hardening by hardware/software co-design on platform FPGAs. In *Proceedings of the 24th Annual International Conference on Application-Specific Systems Architectures and Processors (ASAP'13)*. IEEE, June 2013.

[5] **Andrew G. Schmidt**, John Paul Walters, Matthew French, Didier Keymeulen, Nazeeh Aranki, Matthew Klimesh, and Aaron Kiely. Integrating fast lossless compression prediction with radiation hardening by software on FPGAs. In *Proceedings of the 2012 IEEE Aerospace Conference*. IEEE, March 2012.

[6] **Andrew G. Schmidt** and Ron Sass. Improving design productivity with a hardware performance monitoring infrastructure. In *Proceedings of the 6th Annual International Conference on Reconfigurable Computing and FPGAs (ReConFig'11)*. IEEE Computer Society, November 2011.

[7] William V. Kritikos, Yamuna Rajasekhar, **Andrew G. Schmidt**, and Ron Sass. A radix tree router for scalable FPGA networks. In *Proceedings of the 21th Annual Conference on Field Programmable Logic and Applications (FPL'11)*. IEEE Computer Society, September 2011.

[8] Ron Sass, **Andrew G. Schmidt**, and Scott Buscemi. Reconfigurable computing cluster project: A five-year perspective of the project. In *Parallel Computing with FPGAs (ParaFPGA 2011)*. IEEE Computer Society, August 2011.

[9] **Andrew G. Schmidt**, Bin Huang, Ron Sass, and Matthew French. Checkpoint/restart and beyond: Resilient high performance computing with FPGAs. In *Proceedings of the 19th Annual IEEE Symposium on Field-Programmable Custom Computing Machines (FCCM'11)*, pages 162–169. IEEE Computer Society, May 2011.

[10] **Andrew G. Schmidt**, William V. Kritikos, Ron Sass, Erik K. Anderson, and Matthew French. Merging programming models and on-chip networks to meet the programmable and performance needs of multi-core systems on a programmable chip. In *Proceedings of the 5th Annual International Conference on Reconfigurable Computing and FPGAs (ReConFig'10)*, pages 334–339. IEEE Computer Society, December 2010. [*Best Paper Award Winner*].

[11] Shanyuan Gao, **Andrew G. Schmidt**, and Ron Sass. Impact of reconfigurable hardware on accelerating `MPI_Reduce`. In *Proceedings of the 9th Annual International Conference on Field Programmable Technology (FPT'10)*, pages 29–36. IEEE Computer Society, December 2010.

[12] Bin Huang, **Andrew G. Schmidt**, Ashwin A. Mendon, and Ron Sass. Investigating resilient high performance reconfigurable computing with minimally-invasive system monitoring. In *International Workshop on High-Performance Reconfigurable Computing Technology and Applications (HPRCTA'10)*, pages 1–8. IEEE Computer Society, November 2010. [*OpenFPGA Award Winner*].

[13] **Andrew G. Schmidt**, Siddhartha Datta, Ashwin A. Mendon, and Ron Sass. Productively scaling i/o bound streaming applications with a cluster of FPGAs. In *Symposium on Application Accelerators in High-Performance Computing (SAAHPC'10)*, July 2010.

[14] Shanyuan Gao, **Andrew G. Schmidt**, and Ron Sass. Hardware implementation of mpi_barrier on an FPGA cluster. In *Proceedings of the 19th Annual Conference on Field Programmable Logic and Applications (FPL'09)*, pages 12–17. IEEE Computer Society, September 2009.

[15] **Andrew G. Schmidt**, William V. Kritikos, Rahul R. Sharma, and Ron Sass. AIREN: A novel integration of on-chip and off-chip FPGA networks. In *Proceedings of the 17th Annual IEEE Symposium on Field-Programmable Custom Computing Machines (FCCM'09)*, pages 271–274. IEEE Computer Society, April 2009.

[16] Yamuna Rajasekhar, William V. Kritikos, **Andrew G. Schmidt**, and Ron Sass. Teaching FPGA system design via a remote laboratory facility. In *Proceedings of the 18th Annual Conference on Field Programmable Logic and Applications (FPL'08)*, pages 687–690. IEEE Computer Society, September 2008.

[17] **Andrew G. Schmidt** and Ron Sass. Characterizing effective memory bandwidth of designs with concurrent high-performance computing cores. In *Proceedings of the 17th Annual International Conference on Field Programmable Logic and Applications (FPL'07)*, pages 601–604. IEEE Computer Society, August 2007.

[18] Ron Sass, William V. Kritikos, **Andrew G. Schmidt**, Srinivas Beeravolu, Parag Beeraka, Kushal Datta, David Andrews, Richard S. Miller, and Jr. Daniel Stanzione. Reconfigurable computing cluster (RCC) project: Investigating the feasibility of FPGA-based petascale computing. In *Proceedings of the 15th Annual IEEE Symposium on Field-Programmable Custom Computing Machines (FCCM'07)*, pages 127–140. IEEE Computer Society, April 2007.

Posters and Abstracts

[1] William V. Kritikos, **Andrew G. Schmidt**, Ron Sass, Erik K. Anderson, Michel Sika, and Matthew French. Redsharc: An Abstract Stream Programming Model for FPGAs. In *Proceedings of the 18th Annual IEEE Symposium on Field-Programmable Custom Computing Machines (FCCM'10)*. IEEE Computer Society, May 2010.

[2] Ashwin Mendon, **Andrew G. Schmidt**, and Ron Sass. Initial Implementation of a Hardware File System with Multiple Disk Support. In *Proceedings of the 17th Annual IEEE Symposium on Field-Programmable Custom Computing Machines (FCCM'09)*. IEEE Computer Society, April 2009.

[3] Yamuna Rajasekhar, Yashodhan Phatak, **Andrew G. Schmidt**, William V. Kritikos, and Ron Sass. FPGA Session Control (FSC): Providing Remote Access to A Cluster of FPGAs. In *Proceedings of the 16th Annual IEEE Symposium on Field-Programmable Custom Computing Machines (FCCM'08)*, pages 289–299. IEEE Computer Society, April 2008.

[4] **Andrew G. Schmidt**, William V. Kritikos, Siddhartha Datta, and Ron Sass. Reconfigurable Computing Cluster Project: Phase I Brief. In *Proceedings of the 16th Annual IEEE Symposium on Field-Programmable Custom Computing Machines (FCCM'08)*, pages 300–301. IEEE Computer Society, April 2008.

[5] **Andrew G. Schmidt** and Ron Sass. Quantifying Effective Memory Bandwidth of Platform FPGAs. In *Proceedings of the 15th Annual IEEE Symposium on Field-Programmable Custom Computing Machines (FCCM'07)*, pages 337–338. IEEE Computer Society, April 2007.