Independent Functional Testing of Commercial FPGA Devices

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I. Introduction

The University of Southern California, Information Sciences Institute (USC/ISI) is an applied R&D Institute that serves primarily Government & DoD customers. It was created by DARPA over 40 years ago as a fully captive R&D organization and has since expanded to serving a wide range of customers. USC/ISI has the ability to perform both ITAR and classified work depending on the needs of specific Programs. USC/ISI has operated The MOSIS Foundry Broker Service for over 30 years, which provides Multi-Project Wafers (MPWs), that enable an efficient, affordable path for small volume IC designs on modern semiconductor processes and foundries [1]. USC/ISI has also recently established the SecUre and Robust Electronics (SURE) Center, which focuses on research and development in the areas of trust, security, resiliency and reliability, recognizing over $70M of research in these areas over the past decade.

The combined partnering of the SURE Center and the MOSIS Service Center, provides an in house end-to-end DMEA Accredited Supplier chain from Design, Broker, to Aggregation & Fabrication. It also provides a mechanism whereby successful state of the art government research in these areas can be rapidly matured into industry-relevant solutions. Examples of research in the process of being matured into solutions include 1) "Split Fabrication" technology to obfuscate designs while leveraging off-shore SOA fabrication technology, 2) Reliability assessment of foundry runs through appropriate test coupons & models, and 3) Independent functional testing of FPGA devices. This paper presents an overview of this last item as it is currently transitioning to a solution.

II. FPGA Functional Testing Background

Functional testing of commercial FPGAs, independent of in-house FPGA vendor production testing, is an important first step in establishing a trusted supply-chain, determining the usability of devices stored in inventory for long periods of time, and for determining the health status of fielded systems. While current and next-generation FPGAs are increasingly using emerging technology to thwart counterfeiting attempts, older FPGA generations are easily recycled and sold as new. Devices in deep storage may not have been stored properly, and devices under heavy use or in strenuous operating environments may experience wear out effects. Independent functional testing of the FPGA VLSI provides a sanity check that the device is in fact the device it claims to be and is in good working order. This is no trivial feat as modern FPGA devices now contain over 1B transistors, over a dozen types of Hard IP, 35M user wires, and 380M user routing switches.

[1] www.mosis.com

III. Independent FPGA Functional Testing (IFT) Tools

The USC/ISI IFT tools generate independent functional tests that can be used to cross-check the FPGA manufacturer's testing and can also be used for field testing of counterfeit, damaged, or aging parts. The ability to develop such tests relies upon exhaustive knowledge of the internal FPGA architecture. IFT provides such knowledge for all Xilinx FPGAs dating back to the original Virtex series, and allows automation of the test generation process. IFT currently supports the Xilinx 7-Series architectures (Virtex7, Kintex7, Artix7, Zynq700). Additional architectures can be added with a simple one-time porting effort. Support for any given architecture includes all devices within that architecture.

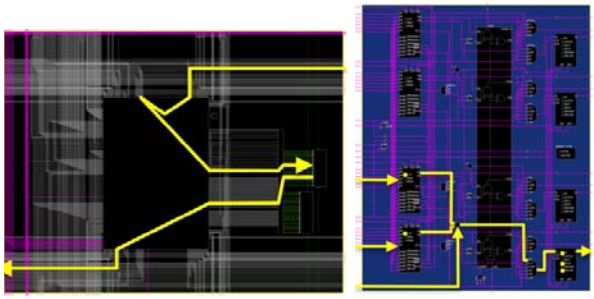

Figure 1 a) Interconnect Testing b) Logic Testing

IFT utilizes stuck-at fault modeling, and covers the configuration memory, the user logic, and the user interconnect. Interconnect testing utilizes custom, massively replicatable paths to exercise user wires and routing multiplexers. Logic is tested using launch and capture of test signals through all paths of configurable logic. IFT leverages regularity, parallelism, and partial reconfiguration to provide a tractable and scalable testing solution. Testing on the largest Virtex7 Zynq (XC7X980T) is performed in less than 1 minute.

IFT provides test coverage metrics that detail exactly which resources are tested, providing a level of confidence to the user. Typical coverage is 95+% of the interconnect, 100% of the SLICE logic, and 90% of the configuration bits. Additional research and development to isolate the remaining resources is expected to yield 100% interconnect coverage and all logic types.