Jeffrey T. Draper
Research Associate Professor, Ming Hsieh Department of Electrical Engineering
Project Leader, Information Sciences Institute
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RESEARCH INTERESTS

Resilient Computing, Exascale Computing, Memory-Oriented Architectures, 3DIC-Inspired Architectures, Hardware Transactional Memories, Networks-on-Chip, Radiation-Hardening by Design

EDUCATION

UNIVERSITY OF TEXAS, AUSTIN, TX

Ph.D. in Computer Engineering, May 1993, GPA: 4.0/4.0
Thesis: *Efficient Message Transport in Multicomputer Systems*
Supervising Professor: Dr. Joydeep Ghosh

M.S.E. in Computer Engineering, August 1990, GPA: 4.0/4.0
Thesis: *The M-Cache: A Message Cache for Message-Passing Multicomputers*
Supervising Professors: Dr. William Athas and Dr. Joydeep Ghosh

TEXAS A\&M UNIVERSITY, COLLEGE STATION, TX

B.S. in Electrical Engineering, May 1987, GPA: 4.0/4.0
Specialization: Microprocessor Systems

EDUCATION HONORS

Fellowships:
Engineering Foundation 1990 – 1991, Microelectronics & Computer Development 1988 – 1990
Scholarships 1983 – 1987:
McFadden, McDermott, Fasken Foundation, UIL Joe B. Cooke
Honor Societies:
Phi Kappa Phi, Tau Beta Pi, Eta Kappa Nu, Phi Eta Sigma
Awards:
Outstanding Junior in the College of Engineering 1986,
Gathright Academic Excellence Award 1986, Dean's List 1983 – 1987

WORK EXPERIENCE

July 1993 to Present
UNIVERSITY OF SOUTHERN CALIFORNIA
INFORMATION SCIENCES INSTITUTE, MARINA DEL REY, CALIFORNIA
MING HSIEH DEPARTMENT OF ELECTRICAL ENGINEERING, LOS ANGELES, CALIFORNIA

Titles: Research Associate Professor, Project Leader

Supervised the work of PhD and MS graduate students and served on numerous PhD screening, qualifier, and defense committees. Taught EE577B - VLSI Design Projects and designed several projects for use in the course. Directed VLSI efforts of several large-scale DARPA-funded projects, as well as NSF and SRC research projects in extreme-scale, data-intensive, and resilient computing. Developed ASIC test articles for the Trusted Integrated Circuits and Integrity and Reliability in Integrated Circuits programs, ranging from simple floating-point units to 50-million transistor quadcore processors. Contributed to the architecture design of polymorphous computing architectures

and co-led the VLSI implementation of a representative chip in IBM 90nm technology that contained on the order of 100 million gates. Directed the VLSI development of two prototype 64Kbit SRAM chips to demonstrate radiation-hardening-by-design principles. Contributed to the architecture design of processor-in-memory chips (PIM) based on embedded DRAM technology and led the corresponding VLSI implementation efforts that produced two 55-million transistor PIM chips. Refer to Research Projects sections for more details.

January 1991 to May 1993
UNIVERSITY OF TEXAS, AUSTIN, TEXAS
Title: Research Assistant
Developed an analytical model for predicting performance measures of message transport in multicomputers. Devised new schemes for message handling and routing in multicomputers and implemented simulation tools to evaluate the schemes. Performed system administration tasks on IBM RS/6000 workstations.

September 1990 to May 1991
UNIVERSITY OF TEXAS, AUSTIN, TEXAS
Title: Teaching Assistant
Served as a proctor, test administrator, and grader in the class entitled *Fundamentals of Logic Design*. Lectured for introductory sessions and tutored students.

June 1987 to August 1988 and Summer 1986
GENERAL DYNAMICS, FT. WORTH, TEXAS
Titles: Engineer, Engineering Intern
Designed and built MC68000-based single-board computers to serve as control units for various projects. Utilized a CAD system to draw schematics of circuits for avionics tester equipment, and edited simulation software for these testers.

TEACHING

Instructor for the class EE577B - VLSI Design Projects several semesters emphasizing advanced VLSI topics such as packaging, I/O design, thermal issues, interconnect modeling, clock/power distribution, low-energy issues, and the use of an industry-standard ASIC design tool flow. Worked with TAs to develop projects to serve as design examples in the class, including tiled quadcore processors, pipelined processors, floating-point units, multimedia extension units, and network-on-chip routing components. Instructor ratings: Spring 2001 4.16/5, Fall 2002 NA, Spring 2004 4.62/5, Spring 2005 4.46/5, Fall 2006 4.1/5, spring 2007 4.3/5, Spring 2010 4.31/5, Spring 2012 4.67/5, Spring 2013 4.17/5.

STUDENT ADVISING

Current/Recent PhD Students Supervised

Lihang Zhao, defended April 2014
Gopi Neela, defended November 2014
Saurabh Hukerikar, qualifier Fall 2013, defense expected Spring 2015
David Lee, qualifier October 2014, defense expected Spring 2016
Aditya Deshpande, screening Spring 2011, qualifier expected Spring 2015
Praveen Sharma, screening Spring 2013, qualifier expected Fall 2015

Former PhD Students Supervised

Dr. Fatemeh Kashfi, Dr. Woojin Choi, Dr. Mahta Haghi, Dr. Bilal Zafar, Dr. Young Hoon Kang, Dr. Taek-Jun Kwon, Dr. Rashed Bhatti, Dr. Riaz Naseer, Dr. Sumit Mediratta, Dr. Jay Moon, Dr. Chang Woo Kang, Dr. Ihn Kim, Dr. Herming Chiueh, Dr. Louis Luh

Former MS Students Supervised
Gregory Lou (MS Thesis), Ravinder Singh, Sachit Chandra, Gokhan Daglikoca, Yamini Kaur, Junaid Qazi, Amit Kapur, Ramanand Venkata

Other Advising
Participated on numerous screening, qualifier, and defense committees including the following students in 2014: Lihang Zhao (defense, Chair), Gopi Neela (defense, Chair), David Lee (qual, Chair), Mohammad Abdel-Majeed (qual), Sang Wook Do (qual), Andrea Sanny (qual); supervised many other students in directed research projects in past years

OTHER RESEARCH ACTIVITIES / SERVICE

2014 Specific Activities: Organized and hosted the Design for Security Workshop involving around 40 attendees from academia, industry, and government agencies; Participated in Exascale Grand Challenge (XGC) External Advisory Board and team meetings at Sandia; Workshop on Near-Data Processing program committee member. Conference interactions at GOMACTech, IPDPS, ISCAS, ISVLSI, MWSCAS, SC; Presented talks at Sandia, DARPA IRIS PI meetings, MWSCAS, and for a number of visitors to ISI and USC. Contributed to the organization of the *Abstracted Interface and Protocol for HPC integration* birds-of-a-feather session at SC; Participated in USC faculty recruiting activities; Participated in the Ming Hsieh Institute Research Festival; Member of the Viterbi School of Engineering Faculty Council; Member of the Information Sciences Institute Security Council; Attained DMEA Trust Certification for chip design activities.

Prior and ongoing activities: Reviewed numerous articles for many journals including *IEEE Transactions on Circuits and Systems*, *IEEE Transactions on Computers*, *IEEE Transactions on Parallel and Distributed Systems*, *Journal of Parallel and Distributed Computing*, *ACM Transactions on Design Automation of Electronic Systems*, and numerous conferences. Reviewed a tutorial for IEEE Computer Society Press. Served on program committees and chaired sessions at many conferences. Served on National Science Foundation proposal review panels. Conducted 2-day short course on Processing-in-Memory (PIM) technology at National Chiao Tung University. Reviewed proposals for the ISI research initiative program.

AFFILIATIONS

IEEE Senior Member, IEEE Computer Society, Tau Beta Pi, Eta Kappa Nu

JOURNAL PUBLICATIONS

- F. Kashfi and J. Draper, "Thermal Sensor Allocation for 3DICs using Three Dimensional Thermal Sensors," *Microelectronics Journal*, vol. 45, iss. 5, pp. 500-507, 2014.
- Woojin Choi, Jeffrey Draper, "Improving Utilization of Hardware Signatures in Transactional Memory," to appear in *Transactions on Parallel and Distributed Processing*, Vol. 24, Iss. 11, pp. 2230-2239, 2013.
- Taek-Jun Kwon, Jeffrey Draper, "Floating-Point Division and Square Root using a Taylor-Series Expansion Algorithm," *Microelectronics Journal*, Vol 40, Number 11, November 2009, pp. 1601 - 1605
- Michael Bajura, et al, "Models and Algorithmic Limits for an ECC-Based Approach to Hardening Sub-100nm SRAMs," *IEEE Transactions on Nuclear Science*, Vol 54, Number 4, August 2007, pp. 935 - 945
- Sumit Mediratta, Jeffrey Draper, "Achieving On-chip Fault-tolerance Utilizing BIST Resources," *WSEAS Transactions on Circuits and Systems*, Vol 5, No 12, December 2006, pp. 1726 – 33

- Jeffrey Draper, et al, "A Prototype Processing-In-Memory (PIM) Chip for the Data-Intensive Architecture (DIVA) System," *Journal of VLSI Signal Processing*, Vol 40, No 1, May 2005, pp. 73 – 84
- Joong-Seok Moon, et al, "Voltage-Pulse Driven Harmonic Resonant Rail Drivers for Low-Power Applications," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, Vol 11/5, October 2003, pp. 762 – 77
- Herming Chiueh, Jeffrey Draper, John Choma, Jr., "A Dynamic Thermal Management Circuit for System-On-Chip Designs," *Analog Integrated Circuits and Signal Processing*, Vol 36/1-2, July - August 2003, pp. 175 – 81
- Herming Chiueh, Jeffrey Draper, John Choma, Jr., "A Programmable Thermal Management Interface Circuit for PowerPC Systems," *Microelectronics Journal*, Vol 32/10-11, pp. 875 - 81
- Louis Luh, John Choma, Jr., and Jeffrey Draper, "A High-Speed Fully Differential Current Switch," *IEEE Transactions on Circuits and Systems*, April 2000, pp. 358 – 63
- Louis Luh, John Choma, Jr., and Jeffrey Draper, "A Continuous-Time Common-Mode Feedback Circuit (CMFB) for High-Impedance Current-Mode Applications," *IEEE Transactions on Circuits and Systems*, April 2000, pp. 363 – 9
- Jeffrey T. Draper and Joydeep Ghosh, "A Comprehensive Analytical Model for Wormhole Routing in Multicomputer Systems," *Journal of Parallel and Distributed Computing*, November 1994, pp. 202 – 14
- Jeffrey T. Draper and Joydeep Ghosh, "The M-Cache: A Message-Handling Mechanism for Multicomputer Systems," *Parallel Computing*, September 1994, pp. 1269 – 88
- Joydeep Ghosh, Kelvin Goveas, and Jeffrey T. Draper, "Performance Evaluation of a Parallel I/O Subsystem for a Hypercube Multicomputer," *Journal of Parallel and Distributed Computing*, January 1993, pp. 190 – 206

CONFERENCE PAPERS/PRESENTATIONS

- L. Zhao and J. Draper, "Consolidated Conflict Detection for Hardware Transactional Memory," in Parallel Architecture and Compilation Techniques, 2014 23rd International Conference on, 2014.
- G. Neela and J. Draper, "A multi-mode energy-efficient double-precision floating-point multiplier," in Circuits and Systems (MWSCAS), 2014 IEEE 57th International Midwest Symposium on, 2014, pp. 29-32.
- D. Lee and J. Draper, "A Framework to Quantify FPGA Design Hardness Against Radiation-Induced Single Event Effects," in Circuits and Systems (MWSCAS), 2014 IEEE 57th International Midwest Symposium on, 2014, pp. 302-305.
- G. Neela and J. Draper, "Modeling the Impact of TSVs on Average Wire Length in 3DICs Using a Tier-Level Hierarchical Approach," in VLSI (ISVLSI), 2014 IEEE Computer Society Annual Symposium on, 2014, pp. 154-159.
- G. Neela and J. Draper, "Optimal techniques for assigning inter-tier signals to 3D-vias with path control in a 3DIC," in Circuits and Systems (ISCAS), 2014 IEEE International Symposium on, 2014, pp. 802-805.
- L. Zhao, L. Chen, and J. Draper, "Mitigating the Mismatch between the Coherence Protocol and Conflict Detection in Hardware Transactional Memory," in Parallel and Distributed Processing Symposium, 2014 IEEE 28th International, 2014, pp. 605-614.
- A. Deshpande and J. Draper, "Cross-layer Analysis of Energy Implications in the Processor/Memory Hierarchy," *Proceedings of the IEEE 28th International Parallel Distributed Processing Symposium (IPDPS)*, PhD Forum, 2014
- A. Deshpande and J. Draper, "Leakage Energy Estimates for HPC Applications," in *Proceedings of the 1st International Workshop on Energy Efficient Supercomputing*, 2013.

- A. Deshpande and J. Draper, "Quantifying the Dominance of Leakage Energy in Large-Scale System Caches," in *Proceedings of the International Conference on High Performance Computing, Networking, Storage and Analysis*, 2013.
- L. Zhao, L. Chen, and J. Draper, "PUNO: Predictive Unicast and Notification to Mitigate the Mismatch between Coherence Protocol and Conflict Detection in HTM," in *Proceedings of the International Conference on High Performance Computing, Networking, Storage and Analysis*, 2013, Best Poster Finalist
- G. Neela and J. Draper, "Techniques for Assigning Inter-Tier Signals to Bondpoints in a Face-to-Face Bonded 3DIC," in *Proceedings of the IEEE International 3D Systems Integration Conference*, 2013.
- G. Neela and J. Draper, "An asymmetric adaptive-precision energy-efficient 3DIC multiplier," in *Proceedings of the 23rd ACM international conference on Great lakes symposium on VLSI*, 2013, pp. 269-274.
- F. Kashfi and J. Draper, "Multiobjective Optimization of Cost, Performance and Thermal Reliability in 3DICs," in 2013 Euromicro Conference on Digital System Design (DSD), 2013, pp. 404-411.
- L. Zhao and J. Draper, "Implementation of hybrid version management in hardware transactional memory," in *Proceedings of the 2013 IEEE International Symposium on Circuits and Systems (ISCAS)*, 2013, pp. 777-780.
- G. Neela and J. Draper, "Logic-on-logic partitioning techniques for 3-dimensional integrated circuits," in *Proceedings of the 2013 IEEE International Symposium on Circuits and Systems (ISCAS)*, 2013, pp. 789-792.
- L. Zhao, W. Choi, L. Chen, and J. Draper, "In-network traffic regulation for Transactional Memory," in *Proceedings of the 2013 IEEE 19th International Symposium on High Performance Computer Architecture (HPCA)*, 2013, pp. 520-531.
- W. Choi, L. Zhao, and J. Draper, "Mileage-Based Contention Management in Transactional Memory," *Proceedings of the 21st International Conference on Parallel Architectures and Compilation Techniques*, 2012, pp. 471-472
- L. Zhao, W. Choi, and J. Draper, "TMNOC: A Case of HTM and NoC Co-Design for Increased Energy Efficiency and Concurrency," *Proceedings of the 21st International Conference on Parallel Architectures and Compilation Techniques*, pp. 439-440
- F. Kashfi and J. Draper, "Thermal Sensor Distribution Method for 3D Integrated Circuits using Efficient Thermal Map Modeling," in 2012 18th International Workshop on Thermal Investigations of ICs and Systems (THERMINIC), 2012, pp. 1-6
- A. Deshpande and J. Draper, "Comparing Squaring and Cubing Units with Multipliers," *Proceedings of the IEEE 55th International Midwest Symposium on Circuits and Systems (MWSCAS)*, 2012, pp. 466-469
- F. Kashfi and J. Draper, "Thermal Sensor Design for 3D ICs," *Proceedings of the IEEE 55th International Midwest Symposium on Circuits and Systems (MWSCAS)*, 2012, pp. 482-485.
- G. Neela and J. Draper, "Challenges in 3DIC Implementation of a Design using Current CAD Tools," *Proceedings of the IEEE 55th International Midwest Symposium on Circuits and Systems (MWSCAS)*, 2012, pp. 478-481
- L. Zhao, W. Choi, and J. Draper, "SEL-TM: Selective Eager-Lazy Management for Improved Concurrency in Transactional Memory," *Proceedings of the IEEE 26th International Parallel Distributed Processing Symposium (IPDPS)*, 2012, pp. 95-106
- L. Zhao and J. Draper, "On the Correctness of Mixing Lazy and Eager Version Management in Transactions," *Proceedings of the IEEE 26th International Parallel Distributed Processing Symposium (IPDPS)*, PhD Forum, 2012, pp. 2534-2537

- Woojin Choi and Jeff Draper, Implementation of Unified Signatures for Transactional Memory Systems, *Proceedings of the IEEE International Midwest Symposium on Circuits and Systems*, August 2011
- Mahta Haghi and Jeff Draper, Single-Event Transient Mitigation in Sub-micron Combinational Circuits, *Proceedings of the IEEE International Midwest Symposium on Circuits and Systems*, August 2011
- Mahta Haghi and Jeff Draper, Comparison of Charge Sharing Reduction Techniques in Deep Sub-micron CMOS Processes, *Proceedings of the IEEE International Midwest Symposium on Circuits and Systems*, August 2011
- Woojin Choi and Jeff Draper, Unified Signatures for Improving Performance in Transactional Memory, *Proceedings of the 25th IEEE International Parallel and Distributed Processing Symposium*, May 2011
- Bilal Zafar, Jeff Draper, Timothy Pinkston, "Cubic Ring Networks: A Polymorphic Topology for Network-on-Chip," *Proceedings of the International Conference on Parallel Processing*, September 2010
- Young Hoon Kang, Jeff Draper, "Fault-Tolerant Flow Control for Control Circuitry in On-Chip Routers," TECHCON 2010, September 2010
- Aditya Deshpande and Jeff Draper, "Squaring Units and a Comparison with Multipliers," *Proceedings of the IEEE International Midwest Symposium on Circuits and Systems*, August 2010
- Mahta Haghi and Jeff Draper, A Single-Event Upset Hardening Technique for High Speed MOS Current Mode Logic, *Proceedings of the IEEE International Symposium on Circuits and Systems*, June 2010
- Woojin Choi, Young Hoon Kang, Taek-Jun Kwon, Jeff Draper, Implementation of Adaptive Grain Signatures for Transactional Memories, *Proceedings of the IEEE International Symposium on Circuits and Systems*, June 2010
- Young Hoon Kang, Taek-Jun Kwon, Jeff Draper, Fault-Tolerant Flow Control in On-Chip Networks, *Proceedings of the 4th ACM/IEEE International Symposium on Networks-on-Chip*, May 2010
- Woojin Choi and Jeff Draper, Locality-Aware Adaptive Grain Signatures for Transactional Memories, *Proceedings of the 24th IEEE International Parallel and Distributed Processing Symposium*, April 2010
- Mahta Haghi and Jeff Draper, The 90 nm Double-DICE Storage Element to Reduce Single-Event Upsets, *Proceedings of the IEEE International Midwest Symposium on Circuits and Systems*, August 2009, pp. 463 – 466
- Young Hoon Kang, Jeff Sondeen, Jeff Draper, Implementing Tree-Based Multicast Routing for Write Invalidation Messages in Networks-on-Chip, *Proceedings of the IEEE International Midwest Symposium on Circuits and Systems*, August 2009, pp. 1118 – 1121
- Young Hoon Kang, Taek-Jun Kwon, Jeff Draper, Dynamic Packet Fragmentation for Increased Virtual Channel Utilization in On-Chip Routers, *Proceedings of the 3rd ACM/IEEE International Symposium on Networks-on-Chip*, May 2009
- Mahta Haghi and Jeff Draper, The Effect of Design Parameters on Single-Event Upset Sensitivity of MOS Current Mode Logic, *Proceedings of the 2009 ACM Great Lakes Symposium on VLSI*, May 2009, pp. 233 - 238
- Young Hoon Kang, Jeff Sondeen, Jeff Draper, Multicast Routing with Dynamic Packet Fragmentation, *Proceedings of the 2009 ACM Great Lakes Symposium on VLSI*, May 2009, pp. 113 - 116
- Riaz Naseer and Jeff Draper, Parallel Double Error Correcting Code Design to Mitigate Multi-Bit Upsets in SRAMs, *Proceedings of the European Solid-State Circuits Conference*, September 2008, pp. 222 - 225

- Taek-Jun Kwon, Jeff Sondeen, Jeff Draper, Floating-Point Division and Square Root Implementation using a Taylor-Series Expansion Algorithm, *Proceedings of the IEEE International Conference on Electronics, Circuits and Systems*, September 2008, pp. 702 – 705
- Riaz Naseer and Jeff Draper, DEC ECC Design to Improve Memory Reliability in Sub-100nm Technologies, *Proceedings of the IEEE International Conference on Electronics, Circuits and Systems*, September 2008, pp. 586 - 589
- Riaz Naseer, et al, Single-Event Effects Characterization and Soft Error Mitigation in 90nm Commercial-Density SRAMs, *Proceedings of the IASTED International Conference on Circuits and Systems*, August 2008, pp. 153 - 158
- Taek-Jun Kwon, Jeff Draper, Floating-Point Division and Square Root Implementation using a Taylor-Series Expansion Algorithm with Reduced Look-up Tables, *Proceedings of the IEEE International Midwest Symposium on Circuits and Systems*, August 2008, pp. 954 - 957
- Young Hoon Kang, Jeffrey Draper, Precise Exception Handling in Discontinuous Control Flow Scenarios for Area-Constrained Systems, *Proceedings of the IEEE International Midwest Symposium on Circuits and Systems*, August 2008, pp. 527 - 530
- Taek-Jun Kwon, Jeff Sondeen, Jeffrey Draper, Floating-Point Division and Square Root using a Taylor-Series Expansion Algorithm, *Proceedings of the 50th IEEE International Midwest Symposium on Circuits and Systems*, August 2007, pp. 305 - 308
- Young Hoon Kang, Jeffrey Draper, Design Trade-offs for Load/Store Buffers in Embdedded Processing Environments, *Proceedings of the 50th IEEE International Midwest Symposium on Circuits and Systems*, August 2007, pp. 1461 - 1464
- Rashed Zafar Bhatti, Monty Denneau, Jeff Draper, Data Strobe Timing of DDR2 using a Statistical Random Sampling Technique, *Proceedings of the 50th IEEE International Midwest Symposium on Circuits and Systems*, August 2007, pp. 1114 - 1117
- Rashed Zafar Bhatti, Keith Chugg, Jeff Draper, Standard Cell based Pseudo-Random Clock Generator for Statistical Random Sampling of Digital Signals, *Proceedings of the 50th IEEE International Midwest Symposium on Circuits and Systems*, August 2007, pp. 1110 - 1113
- Sumit Mediratta, Jeffrey Draper, Performance Evaluation of Probe-Send Fault-tolerant Network-on-Chip Router, *Proceedings of the IEEE International Conference on Application-Specific Systems, Architectures, and Processors*, July 2007, pp. 69 - 75
- Riaz Naseer, et al, Critical Charge Characterization for Soft Error Rate Modeling in 90nm SRAM, *Proceedings of the IEEE International Symposium on Circuits and Systems*, May 2007, pp. 1879 - 1882
- Sumit Mediratta, Jeffrey Draper, Characterization of a Fault-tolerant NoC Router, *Proceedings of the IEEE International Symposium on Circuits and Systems*, May 2007, pp. 381 - 384
- Riaz Naseer, et al, Critical Charge and SET Pulse Widths for Combinational Logic in Commercial 90nm CMOS Technology, *Proceedings of the 2007 ACM Great Lakes Symposium on VLSI*, March 2007, pp. 227 - 230
- Sumit Mediratta, Jeffrey Draper, Effective Realization of On-chip Fault-tolerance Utilizing BIST Resources, *Proceedings of the 5th WSEAS Int. Conf. on Circuits, Systems, Electronics, Control & Signal Processing*, November 2006
- Riaz Naseer, Rashed Zafar Bhatti, Jeff Draper, Analysis of Soft Error Mitigation Techniques for Register Files in IBM Cu-08 90nm Technology, *Proceedings of the 49th IEEE International Midwest Symposium on Circuits and Systems*, August 2006
- Sumit Mediratta, Jeffrey Draper, On-chip Fault-tolerance Utilizing BIST Resources, *Proceedings of the 49th IEEE International Midwest Symposium on Circuits and Systems*, August 2006
- Rashed Zafar Bhatti, Craig Steele, Jeff Draper, PBuf: An On-Chip Packet Transfer Engine for MONARCH, *Proceedings of the 49th IEEE International Midwest Symposium on Circuits and Systems*, August 2006

- Riaz Naseer, Jeff Draper, DF-DICE: A Scalable Solution for Soft Error Tolerant Circuit Design, *Proceedings of the IEEE International Symposium on Circuits and Systems*, May 2006, pp. 3890 – 3
- Rashed Bhatti, Monty Denneau, Jeff Draper, Phase Measurement and Adjustment of Digital Signals Using Random Sampling Technique, *Proceedings of the IEEE International Symposium on Circuits and Systems*, May 2006, pp. 3886 – 9
- Tim Barrett, et al, A Double-Data Rate (DDR) Processing-in-Memory (PIM) Device with WideWord Floating-Point Capability, *Proceedings of the IEEE International Symposium on Circuits and Systems*, May 2006, pp. 1933 – 6
- Rashed Zafar Bhatti, Monty Denneau, Jeff Draper, 2 Gbps SerDes Design Based on IBM Cu-11 (130nm) Standard Cell Technology, *Proceedings of the 2006 ACM Great Lakes Symposium on VLSI*, May 2006, pp. 198 – 203
- Sumit Mediratta, Jeffrey Draper, Performance Analysis of User-Level PIM Communication in the Data-Intensive Architecture (DIVA) System, *Proceedings of the 12th International Conference on High Performance Computing (HiPC 2005)*, December 2005, pp. 407 – 19
- Rashed Zafar Bhatti, Monty Denneau, Jeff Draper, Duty Cycle Measurement and Correction Using a Random Sampling Technique, *Proceedings of the 48th IEEE International Midwest Symposium on Circuits and Systems*, August 2005
- Riaz Naseer, Jeff Draper, The DF-DICE Storage Element for Immunity to Soft Errors, *Proceedings of the 48th IEEE International Midwest Symposium on Circuits and Systems*, August 2005
- Taek-Jun Kwon, Jeff Sondeen, Jeff Draper, Design Trade-Offs in Floating-Point Unit Implementation for Embedded and Processing-In-Memory Systems, *Proceedings of the IEEE International Symposium on Circuits and Systems*, May 2005, pp. 3331 – 4
- Sumit Mediratta, Craig Steele, Jeff Sondeen, Jeffrey Draper, An Area-Efficient and Protected Network Interface for Processing-In-Memory Systems, *Proceedings of the IEEE International Symposium on Circuits and Systems*, May 2005, pp. 2951 – 4
- Sumit Mediratta, Craig Steele, Ravinder Singh, Jeff Sondeen, Jeffrey Draper, A 0.18um CMOS Implementation of an Area Efficient Precise Exception Handling Unit for Processing-In-Memory Systems, *Proceedings of the 47th IEEE International Midwest Symposium on Circuits and Systems*, July 2004, Vol. III, pp. 455 – 58
- Taek-Jun Kwon, Joong-Seok Moon, Jeff Sondeen, Jeff Draper, A 0.18um Implementation of a Floating-Point Unit for a Processing-In-Memory System, *Proceedings of the IEEE International Symposium on Circuits and Systems*, May 2004, Vol. II, pp. 453 – 56
- Sumit Mediratta, Jeff Sondeen, Jeffrey Draper, An Area-Efficient Router for the Data-Intensive Architecture (DIVA) System, *Proceedings of the 17th International Conference on VLSI Design* , January 2004
- Joong-Seok Moon, Taek-Jun Kwon, Jeff Sondeen, Jeff Draper, An Area-Efficient Standard-Cell Floating-Point Unit Design for a Processing-In-Memory System, *Proceedings of the 29th European Solid-State Circuit Conference* , September 2003
- Jeffrey Draper, Jeff Sondeen, Chang Woo Kang, Implementation of a 256-bit WideWord Processor for the Data-Intensive Architecture (DIVA) Processing-In-Memory (PIM) Chip, *Proceedings of the 28th European Solid-State Circuit Conference* , September 2002
- Herming Chiueh, Jeffrey Draper, Sumit Mediratta, Jeff Sondeen, The Address Translation Unit of the Data-Intensive Architecture (DIVA) System, *Proceedings of the 28th European Solid-State Circuit Conference* , September 2002
- Jeffrey Draper, Jeff Sondeen, Sumit Mediratta, Ihn Kim, Implementation of a 32-bit RISC Processor for the Data-Intensive Architecture Processing-In-Memory Chip, *Proceedings of the IEEE International Conference on Application-Specific Systems, Architectures, and Processors*, July 2002

- Jeff Draper, et al, The Architecture of the DIVA Processing-In-Memory Chip, *Proceedings of the International Conference on Supercomputing*, June 2002
- Joong-Seok Moon, William C. Athas, Peter A. Beerel, Jeffrey T. Draper, Low-Power Sequential Access Memory Design, *Proceedings of the IEEE Custom Integrated Circuits Conference*, May 2002
- Herming Chiueh, Jeffrey Draper, John Choma, Jr., A Dynamic Thermal Management Circuit for System-on-Chip Designs, *Proceedings of the International IEEE Conference on Electronics, Circuits, and Systems*, September 2001
- Herming Chiueh, Jeffrey Draper, John Choma, Jr., A Thermal Management System and Prototyping for System-on-Chip Designs, *Proceedings of the 2001 Southwest Symposium on Mixed-Signal Design*, February 2001
- Herming Chiueh, Jeffrey Draper, John Choma, Jr., A Programmable Thermal Management Interface Circuit for PowerPC Systems, *Proceedings of the 6th International Workshop on Thermal Investigation of ICs and Systems*, September 2000
- Louis Luh, John Choma, Jr., Jeffrey Draper, A 400MHz 5th-Order CMOS Continuous-Time Switched-Current Sigma-Delta Modulator, *Proceedings of the European Solid-State Circuits Conference*, September 2000
- Herming Chiueh, Jeffrey Draper, and John Choma, Jr., Implementation of a Temperature Monitoring Interface Circuit for PowerPC Systems *Proceedings of the IEEE Midwest Symposium on Circuits and Systems*, August 2000
- Chang Woo Kang and Jeffrey Draper, A Fast, Simple Router for the Data-Intensive Architecture (DIVA) System, *Proceedings of the IEEE Midwest Symposium on Circuits and Systems*, August 2000
- Louis Luh, Jeffrey Draper, and John Choma, Jr., Performance Optimization for High-Order Continuous-Time Sigma-Delta Modulators with Extra Loop Delay, *Proceedings of the IEEE International Symposium on Circuits and Systems*, May 2000
- Louis Luh, Jeffrey Draper, and John Choma, Jr., A Zener-Diode-Activated ESD Protection Circuit for Sub-Micron CMOS Processes, *Proceedings of the IEEE International Symposium on Circuits and Systems*, May 2000
- Herming Chiueh, Jeffrey Draper, and John Choma, Jr., A Novel Fully Integrated Fan Controller for Advanced Computer Systems *Proceedings of the Southwest Symposium on Mixed-Signal Design*, February 2000
- Mary Hall, et al, Mapping Irregular Applications to DIVA, a PIM-based Data-Intensive Architecture, *Proceedings of Supercomputing*, November 1999
- Louis Luh, John Choma, Jr., Jeffrey Draper, Herming Chiueh, A High-Speed CMOS On-Chip Temperature Sensor, *Proceedings of the European Solid-State Circuits Conference*, September 1999, pp 290 – 3
- Louis Luh, John Choma, Jr., Jeffrey Draper, Herming Chiueh, A High-Speed Digital Comb Filter for Sigma-Delta Analog-to-Digital Conversion, *Proceedings of the IEEE Midwest Symposium on Circuits and Systems*, August 1999
- Louis Luh, John Choma, Jr., and Jeffrey Draper, Circuit Design Challenges for High-Speed CMOS Continuous-Time Switched-Current Sigma-Delta Modulators, *Proceedings of the IEEE Midwest Symposium on Circuits and Systems*, August 1999
- Louis Luh, Jeffrey Draper, and John Choma, Jr., A Self-Sensing Tristate Pad Driver for Control Signals of Multiple Bus Controllers, *Proceedings of the IEEE International Symposium on Circuits and Systems*, May 1999
- Louis Luh, John Choma, and Jeffrey Draper, Area-Efficient Area Pad Design for High Pin-Count Chips, *Proceedings of the Great Lakes Symposium on VLSI*, March 1999, pp. 78 – 81

- Herming Chiueh, Jeffrey Draper, Louis Luh, and John Choma, A Novel Model for On-Chip Heat Dissipation, *Proceedings of the 1998 IEEE Asia-Pacific Conference on Circuits and Systems*, November 1998, pp. 779 – 82
- Louis Luh, John Choma, and Jeffrey Draper, A Continuous-Time Common-Mode Feedback Circuit (CMFB) for High-Impedance Current-Mode Application, *Proceedings of the 5th IEEE International Conference on Electronics, Circuits, and Systems*, September 1998, Vol. 3, pp. 347 – 50
- Louis Luh, John Choma, and Jeffrey Draper, A High-Speed Fully Differential Current Switch, *Proceedings of the 5th IEEE International Conference on Electronics, Circuits, and Systems*, September 1998, Vol. 3, pp. 343 – 6
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ACTIVE FUNDED RESEARCH PROJECTS

Integrity and Reliability in Integrated Circuits, DARPA, February 2011 – present
The DARPA Integrity and Reliability in IC program is fostering the development of technology for deriving the functionality of an IC to determine unambiguously if undocumented functionality has been incorporated somewhere along the fabrication chain, and to accurately determine the IC's useful lifespan from a physical perspective. Since ICs are at the core of most systems and provide the critical functionalities that differentiate systems (e.g., detection and signal processing, targeting, and processing), changes such as additions in functionality or intentionally reduced lifespan could cause faulty operation. Our primary task on the program will develop a series of designs/chips that will be used to test the integrity and reliability assessment technology under development by the IRIS program. System-on-chip and multi-core architecture research will be leveraged in the test chip design.

Memory Architectures for Exascale Grand Challenge Problems, Sandia, January 2012 – September 2014
Leveraging their prior work on DARPA's Ubiquitous High Performance Computing (UHPC) program, USC is working with Sandia National Laboratories to address Exascale Grand Challenge (XGC) problems. The goal of the program is to overcome current limiting factors, such as power consumption and architectural and programming complexity, by developing entirely new computer architectures and programming models. The aim is to produce a more energy-efficient computer that delivers 100 to 1,000 times more performance and is easier to program than current systems. USC's role will leverage expertise in processing-in-memory technology to develop energy-efficient and resilient embedded memory processors targeted to 3DIC memory stacks.

COMPLETED RESEARCH PROJECTS

Resilient Computing, SRC / DARPA, November 2009 – January 2013
Exploration of resilient computing techniques is being conducted as part of the Multi-Scale Systems Center (MuSyc), sponsored by MARCO and DARPA under the Focus Center Research Program. MARCO is a wholly-owned subsidiary of the Semiconductor Research Corporation. MuSyc is directed by Jan Rabaey of the University of California at Berkeley. The research is specifically addressing the areas of energy versus resilience trade-offs in fault-tolerant networks-on-chip and memories.

Leading Edge Fabrication Technology Experiments, JPL, September 2012 – August 2013
Through the government-sponsored Trusted Access Program Office fabrication path, a number of experiments are being conducted in collaboration under funding from JPL to study the extent of variation in advanced technology nodes such as IBM's 22nm process.

X-Caliber Ubiquitous High-Performance Computing, Sandia / DARPA, September 2010 – September 2012
USC collaborated with Sandia National Laboratories on the UHPC XCaliber project. Sandia National Laboratories has been selected as one of four institutions to develop new supercomputer prototype systems for DARPA's Ubiquitous High Performance Computing (UHPC) program. The goal of the UHPC program is to overcome current limiting factors, such as power consumption and architectural and programming complexity, by developing entirely new computer architectures and programming models. The aim is to produce a more energy-efficient computer that delivers 100 to 1,000 times more performance and is easier to program than current systems. To accomplish the mission, Sandia Labs is leading a team of industry and academic partners, which includes USC. USC's role will leverage expertise in processing-in-memory technology to develop energy-efficient and resilient embedded memory processors.

Object-Accelerated Computational Fabric, Exogi, LLC / DARPA, November 2010 – August 2012
RISC instruction sets exist because they are easy to decode and pipeline, but they have relatively low information density and operate on similarly primitive data types. However, the codes these CPUs are typically running today are largely object-oriented languages, with either static or dynamic method dispatch. Programmer productivity is a relatively constant number of lines of code per day, whether assembly language or a much higher-level abstraction such as a modern object-based language. The information density and expressivity of an object-oriented language are much greater, and the computational effort induced by each object method invocation can be much greater, than those of conventional languages for which our RISC processors were developed. In response, the OACF project seeks to:

- Raise the level of abstraction in RISC-based hardware by supporting an efficient set of object-oriented hardware features.
- Recognize that data transfer, prefetching, sharing and caching can be vastly more efficient if structural information that is currently discarded when compiling object-oriented programs to RISC instructions can be exploited by low-level hardware elements
- Realize that the ultimate scalability of systems on a chip (SoC) designs requires a revolutionary reduction in network interface overhead, and
- Revamp the processing model to make the central processing unit a coordinator of networked heterogeneous specialist co-processors rather than the primary locus of computation for a whole system.

Radiation Effects on Electronics in Aligned Carbon Nanotube Technology, DTRA, June 2010 – March 2012
CMOS scaling below the 100 nm feature size is increasingly challenging the reliable operation of commercial-process-based electronics in space and strategic radiation environments. Concurrently emerging are carbon-nanotube-based technologies that already exhibit performances rivaling the most advanced CMOS processes while showing a promising inherent resilience to radiation. In consideration of these developments, the RadCNT project is exploring the basic mechanisms and phenomena from ionizing and non-ionizing radiation effects on field-effect transistors and circuits, based on self- aligned carbon nanotube technology. The multi-year effort's objective is to gradually combine TCAD molecular modeling and simulation of CNTs with basic device fabrication and experimental radiation testing, for the purpose of establishing a fundamental understanding of underlying radiation mechanisms and their effects, from basic FET structures to logic gates and ultimately simple integrated circuits.

Trusted in Integrated Circuits, DARPA, October 2007 – February 2012
The DARPA Trust in IC program has observed the trend of foundries and design houses moving off-shore. The program is attempting to develop techniques for guaranteeing that the devices that come back from fabrication identically match the designs submitted, specifically that no "Trojan horses" have been inserted to the design. While obvious national security issues are involved in such a paradigm, in an academic sense, the program involves techniques for demonstrating proofs of correctness. Our primary role on the program is to provide ASIC test chips that can serve as testbeds for demonstrating such techniques. The program is a phased program starting with smaller ASICs and building up to 100M-transistor chips by the final phase. Multi-core and network-on-chip architecture research has been included in the final phases.

Radiation-Hardening-by-Design (RHBD), DARPA, January 2006 – June 2010
The main thrust of the RHBD program is to use architecture, circuit design, and layout techniques to build chips that are radiation-tolerant by using commodity commercial foundry lines. This approach is becoming highly desired because radiation-hard foundries are becoming prohibitively expensive and the technologies they support tend to lag behind state-of-the-art by two or three generations. In initial experiments we have designed 64Kbit SRAM chips using RHBD techniques and have fabricated two

such chips: one in IBM 9LP 90nm technology and the other in IBM 9SF 90nm technology. Radiation tests have shown that these chips perform with respect to single-event effects and are also capable of performing with high total ionizing doses (greater than 300 Krads). Further testing has shown that high-temperature treatments produce an annealing effect that restores previously irradiated chips to their pre-radiated state.

Technology / Hardware Study for an Exascale Point Design Study, NSF, September 2009 – August 2010
With the emergence of Petascale computing systems, the HPC community is engaged in a critical assessment of future performance opportunities, inhibiting challenges, and research directions characterizing the potential accomplishment of Exascale computing systems and their application. More than three orders of magnitude more powerful than today's fastest supercomputers, Exascale class systems will demand innovation in computer technology and design, system software and programming models, and applications and algorithms far beyond current conventional concepts and practices. With the benefit of prior experience and the findings of many community forums addressing Exascale computing, we are evaluating enabling technologies, micro-architectures, and hardware system design for an Exascale point design study. The results of this study will be integrated with those of companion studies in architectures and system software to combat current system deficiencies including latency, starvation, overhead, and contention by better enabling novel techniques of locality management, exposing and exploiting billion-way parallelism, innovative efficient mechanisms for synchronization and context scheduling, and high-throughput structures. Collaborators included Louisiana State University, University of Illinois (UIUC), and Sandia National Laboratory.

Resilient Programming Model and Machine, DoD, October 2008 – December 2009
The practice of large-scale concurrent computing remains an arcane specialty despite the many advances in the underlying communication and computational hardware systems. The clumsiness and complication of existing concurrent programming environments may be the most significant barrier to the productive exploitation of emerging concurrent computing technologies. The other horn of the dilemma of grandly scaled computing systems is the requirement that failed and failing components, inevitable in both software and hardware, must not stymie the overall forward progress of the computation. In this study, we are exploring a simplified but intrinsically fault-tolerant concurrent programming model efficiently supported by resilient transactionally-aware network and network interface hardware. The approach integrates an inherently resilient stateless transactional programming model, which externalizes all data management, with advanced network interface and transport mechanisms capable of autonomous publish-and-subscribe distribution of conventional, streaming and transactional data entities. Fault detection and low-cost replication of essential data on the part of the transactionally-aware network hardware complement the programming model which decouples user-level stateless actors from explicit or fixed hardware bindings.

Morphable Networked Architectures (MONARCH), DARPA, June 2001 – March 2007
The MONARCH project investigated polymorphous computing architectures that can adapt underlying computing structures to perform efficient computing in response to algorithm needs or even stimuli from the environment. The MONARCH architecture will support reactive multi-mission, multi-sensor, and in-flight re-targetable missions. In support of this project, DIVA PIM technology is being integrated with a Raytheon streaming architecture design to implement a polymorphic computing platform. A MONARCH chip measuring almost 19mm on a side has been fabricated in IBM 90nm technology and is currently in laboratory operation at Raytheon. This 100M-gate chip contains six RISC processors with multimedia extension units, 12 MB of embedded DRAM, a 64-GFLOP streaming computing fabric, two external DDR DRAM memory ports, two Rapid I/O ports, and 16 high-speed serial ports.

Cognitive Engine Technologies (COGENT), DARPA, August 2004 - July 2006
COGENT was a multidisciplinary effort to study, develop, and evaluate concepts for an advanced cognitive information processing architecture. The approach of COGENT architecture development exploited advances in problem solving approaches, computer architecture, power management, storage techniques and even relevant new technologies to achieve substantial improvements in cognitive processing throughput.

PIM Technology for Knowledge Discovery, AFRL, August 2004 - November 2005
This project explored the use of processing-in-memory (PIM) technology to speed up algorithms used in knowledge discovery applications. Besides the analysis of algorithms, applications were ported to PIM systems developed under the DIVA and Godiva projects for benchmarking purposes. Based on these performance results, projections incorporating technology roadmaps were formulated to predict capabilities of mature PIM technology.

Cyclops SERDES Design, IBM T. J. Watson, September 2004 - January 2005
The IBM Cyclops project is building a multithreaded architecture for cellular computing. The VLSI devices incorporated in this architecture contain high-speed serial links for interconnecting devices. These links require serializers and deserializers (SERDES) to convert between the on-chip high-speed parallel buses and off-chip high-speed serial links. We developed a fully digital design using a novel random sampling technique to accomplish this requirement in less area and with lower power dissipation than alternatives.

Godiva, DARPA, August 2002 - February 2004
The Godiva project was a collaborative effort between USC, Hewlett-Packard Laboratories, and Rice University to investigate how processing-in-memory (PIM) technology could be applied to commercial systems. This project leveraged research from the Data-Intensive Architecture (DIVA) project. In addition to the basic research component of this project, a prototype system was developed that inserts processing-in-memory (PIM) devices with floating-point capability into the memory system of an HP Long's Peak server, which is based on the Itanium2 processor.

Data-Intensive Architecture (DIVA), DARPA, April 1998 - December 2002
The DIVA project explored the use of embedded DRAM technology to build smart memory coprocessors to a host microprocessor. By also using a separate memory-to-memory interconnect, DIVA exploits inherent bandwidth both on chip and across the system. DIVA supports familiar programming paradigms from parallel computing to target a broad range of applications. The DIVA project built two prototype systems using two different VLSI PIM prototype chips in place of standard DRAMs to demonstrate these concepts. Both prototype PIM chips were fabricated in TSMC 0.18μm technology and contained on the order of 55-million transistors in approximately 100 sq mm. The chips demonstrated an in-system speedup of 35X on an application kernel of interest to DARPA.

Integrated Thermal Management (ITEM), DARPA, October 1995 - June 1999
Innovative techniques for sensing and controlling thermal effects in high density scalable systems were developed, including the investigation of microelectromechanical devices. This capability provides great cost savings in design of a thermal management system for a computer, as it allows a system design that targets nominal power dissipation, rather than worst-case. The resulting system then actively monitors and controls itself to remain within that specification.

Advanced Scalable Network Technology (ASNT), DARPA, October 1995 - September 1999
The ASNT project exploited large numbers of chip pins offered by area pad technology to provide several networks in the same system, each customized for a specific function and/or message type. The idea was formulated from the observation that the message traffic on previous generations of multicomputers

tended to be bimodal: messages were either short control-type messages or large messages for the transfer of huge blocks of data.

Packaging-Driven Scalable System (PDSS), DARPA, October 1994 - June 1997
PDSS is an embeddable multicomputer which utilizes area interconnect to achieve a high-bandwidth 1-dimensional network. This system architecture considerably simplifies interconnect while yielding better performance for systems up to 64 nodes. As part of this project, a custom VLSI chip containing 250,000 transistors and using area pad arrays to provide 555 signals was designed and fabricated. The Red Rover routing algorithm was also developed as part of this project.

Embeddable Variant (EV), DARPA, October 1992 - June 1995
The Embeddable Variant is an adaptation of the Intel Touchstone architecture using multichip module (MCM) technology. The finished system contained 16 nodes in a standard 27 cubic inch SEM-E package. This project involved a wide range of expertise, ranging from ASIC design to operating systems and parallel applications.

Modeling of Wormhole-Routed Networks, 1991 - 1993
An analytical model based on queuing theory principles was developed for yielding latency and throughput measures of wormhole-routed networks. Application of the model to various networks revealed bottlenecks and quantified the effect of cascaded blocking.

MECA (Multi-path E-cube Algorithm), 1990 - 1992
An adaptive routing algorithm based on the dimension-ordered E-cube algorithm was devised. To evaluate the algorithm, a C++ program implementing a detailed network simulator was developed. This simulator was made available to the research community and subsequently used on the ATOMIC design at USC/ISI, which served as the basis of the initial Myricom network router products.

The M-Cache, 1989 - 1990
The M-Cache is a hardware aid for message-driven programming paradigms. This work included hardware design, specification, performance evaluation, and implementation analysis of a technique for speeding up message handling in message-passing multicomputers.

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Available upon request