Duty Cycle Measurement and Correction Using a Random Sampling Technique

Rashed Zafar Bhatti
EE- Systems Department
University of Southern California
Marina del Rey, CA-90292, USA
bhatti@isi.edu

Monty Denneau
IBM T.J. Watson Research Center
Yorktown Heights, NY 10598
denneau@us.ibm.com

Jeff Draper
Information Sciences Institute
University of Southern California
Marina del Rey, CA-90292, USA
draper@isi.edu

***Abstract*— A specific value of duty cycle of an on-chip clock or signal often becomes of extreme significance in VLSI circuits like DRAM's, dynamic/domino pipelined circuits, pipelined analog-to-digital converters (ADC) and Serializer / Deserializer (SERDES) circuits, which are sensitive to the duty cycle or where operations are synchronized with both transitions of the clock. This paper introduces a novel idea based on a random sampling technique of inferential statistics for measurement and local correction of the duty cycle of high-speed on-chip signals. The high measurement accuracy achievable through the proposed random sampling technique provides a way to correct the duty cycle with a maximum error of less than half the smallest delay resolution unit available for correction. An input signal with duty cycle from 30% to 70% can be adjusted to a wide range of values within this range using a purely digital, area-efficient standard cell based design. Our experimental results gathered though extensive simulations of the proposed circuit manifest a very close correlation to the expected theoretical results.**

I. INTRODUCTION

The clock signal is the heart beat for all synchronous digital computing and communication circuits, some of which are sensitive to both edges of the clock. Dynamic and domino logic circuits require one phase of the clock cycle for pre-charge and the other to evaluate, thus imposing a tight constraint on the duty cycle of the clock to operate at maximum possible speed. Memory systems like SRAM's and DRAM's also require a part of the clock cycle to pre-charge the bit/bit bar lines and a part of it for read or write operations [8]. In data communication circuits and systems the importance of clock-to-data correlation is magnified, and large variations in the duty cycle of the clock cannot be tolerated. Similarly, in SERDES technology, when both edges of the serialization signal are used to serialize the data, a balanced duty cycle becomes very important to provide equal transmission time for each symbol. In advanced deep submicron VLSI technologies, the clock is distributed to individual components through a large clock distribution tree made up of clock buffers and interconnects of appropriate sizes to minimize skew and end-to-end delay. A noticeable degradation in duty cycle can be observed at the terminal ends of the signal distribution network, even for signals generated with a perfectly stable and accurate signal source. This is due to the slight mismatch in the drive strengths of pull-up and pull-down networks of the CMOS gates/buffers and non-uniformity in the distribution of wiring capacitance. A local duty cycle correction circuit is usually required to fix this problem.

In this paper, we propose a very simple and novel technique to measure and locally adjust the duty cycle of any clock or signal using a standard cell based circuit design. The proposed circuit exploits the well-known Law of Large Numbers [1] for statistical estimation and repeatedly captures the state of the signal to be measured at random instants of time. A large sample data of premeditated size is gathered that provides the measurement results with an accuracy and confidence level as high as desired. The proposed circuit delays the input signal with a programmable delay line of a modest size; the delayed and original input signals are used to stretch or chop the signal to produce a desired output duty cycle using a small and simple logic circuit. The rest of the paper is organized as follows. Section II discusses some conventional ways to tackle the subject problem. The mapping of statistical estimation theory using random sampling to high-speed on-chip signal measurement is explained in Section III. The subsequent section provides the implementation details along with a brief discussion on random clock generation. Section V shows the experimental results, and Section VI concludes the paper.

II. RELATED WORK

Measurement and correction of duty cycle of on-chip signals is a classic VLSI and ASIC design problem. The design approaches already proposed in the literature can be categorized broadly into analog, digital and mixed-signal. Purely analog duty cycle corrector (DCC) circuits like the one proposed by [6] consist of a voltage controlled oscillator (VCO), operational amplifiers (OPAMP), phase detectors and frequency filters that makes the design extremely resource heavy. These circuits are obviously not a good

choice when die area is the most important constraint. The mixed-signal design approaches [3],[5] are very fast but require very careful design that is independent of process, voltage and temperature variation for analog components like charge pumps, integrators etc. The Synchronous Mirror Delay (SMD) first proposed by [8], forms the basis of digital design approaches like [2],[4]. Although [4] is a pure digital solution of the duty cycle correction problem, it is not an efficient approach, in area and design time, for implementation with standard cell libraries in the ASIC design flow, especially when considerably many DCC's are required all over the chip, and frequent adjustment or relocking is not required. The major hurdles that limit the approach in [4] while working with standard cell libraries are (1) building a custom designed component, like a perfectly symmetric SR flip-flop, (2) building a precisely matched SMD and (3) generating a pulse of a specific width which is a recursive call for the solution. Moreover, the SMD-based designs employ comparatively long delay lines that make the corrected signal more prone to jitter due to power supply variations. The maximum measurement and correction error of [4] is equal to the primary delay element (usually the fastest component in the library) used in the construction of the SMD, whereas the proposed technique provides a way to very accurately measure the duty cycle and reduces the maximum correction error to less than half the smallest delay resolution unit.

III. Theoretical Frame Work

In the proposed technique a random clock is used. The state of the signal to be measured is repeatedly captured at the edge of this random clock. The occurrences of edges of the random clock are assumed to be completely independent of the signal whose duty cycle is to be measured; this implies that it can capture all parts of the signal under measurement with an equal probability. If the duty cycle of the signal is p then the probability of capturing logic high or low in a single trial would be equal to p or $q=(1-p)$,respectively. If X is the number of times logic high is captured at the edge of the random clock in a sample of n trials, from the Law of Large Numbers [1] we have:

$$\lim_{n\to\infty} \frac{X}{n} = p \tag{1}$$

The value of n is kept high and can be premeditated to obtain a certain accuracy and confidence over the observed result. $P=X/n$ is the observed proportion of number of ones captured in a sample of n trials. The probability distribution of this proportion can closely be approximated with a Gaussian distribution, whose mean is $\mu_P=p$ and standard deviation (standard error) $\sigma_P = \sqrt{pq/n}$ [1]. The confidence limit for p is given by the following equation:

$$p = P \pm z_c \sigma_P = P \pm z_c \sqrt{\frac{pq}{n}} = P \pm z_c \sqrt{\frac{p(1-p)}{n}} \tag{2}$$

Where $\pm z_c$ is the critical value that represents the limits within which the area under the bell shaped Gaussian distribution curve is equal to the confidence interval, also known as confidence level. $\pm z_c \sigma_P$ is the standard error in the observed value P. The value $\pm z_c$ for a desired confidence interval CI can be found by $z_c=2½erf\text{-}1(CI)$, and its values are frequently tabulated in literature. The equation (2) can be solved for p in terms of P, z_c and n to get the following equation:

$$p = \left(P + \frac{z_c^2}{2n} \pm z_c \sqrt{\frac{P(1-P)}{n} + \frac{z_c^2}{4n}} \right) \Bigg/ \left(1 + \frac{z_c^2}{n} \right) \tag{3}$$

For a very large value of n the above equation (3) is reduced to the following relation [1]:

$$p \approx P \pm z_c \sqrt{\frac{P(1-P)}{n}} \tag{4}$$

The observed duty cycle can now be mapped to an actual duty cycle with a certain confidence level, and the error $\alpha=(p\text{-}P)$ (the difference of actual and observed value) can be minimized by setting the sample size n using the following formula.

$$n = \left(\frac{z_c}{\alpha} \right)^2 P(1-P) \tag{5}$$

It is obvious from the equation that n has a quadratic relation with accuracy. Fig. 1 shows the relation of sample size with the desired confidence level and tolerable error level for measurement of a signal expected to have 50% duty cycle.

IV. Design Concept And Implementation

The design concept can be understood through the simple block diagram given in Fig. 2. The circuit uses a small programmable delay line that provides a delayed version of the input signal. The delayed signal is ORed with the original input to stretch and ANDed with the input to chop the input signal as illustrated in Fig. 3. This configuration accepts an input duty cycle range of 30% to 70%, and it can adjust a signal with 30% input duty cycle to any desired value within a 30% to 60% range. Similarly a 70% input duty cycle can be adjusted to any desired value within a 40% to 70% range. For example, if the input duty cycle is 30%, a signal that is delayed 20% of the cycle time is ORed with the input to produce a corrected 50% duty cycle.

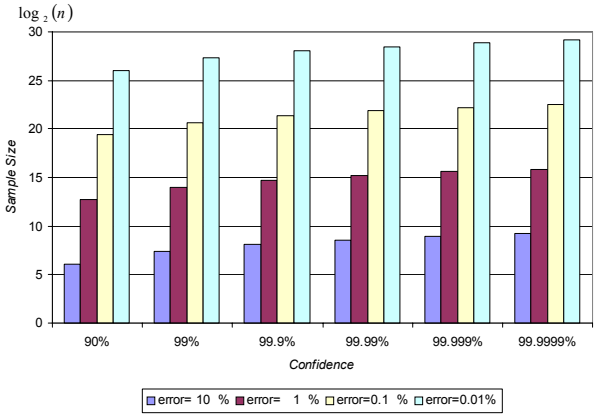

Figure 1. Sample size versus Confidence Level (at $p=.5$).

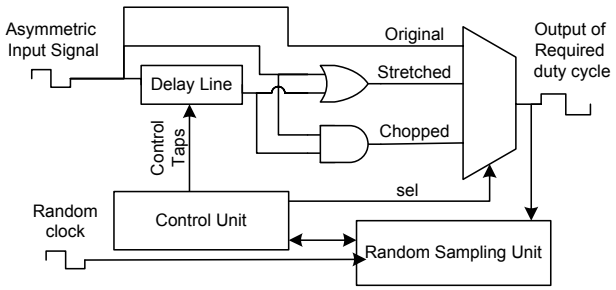

Figure 2. The conceptual diagram of proposed DCC.

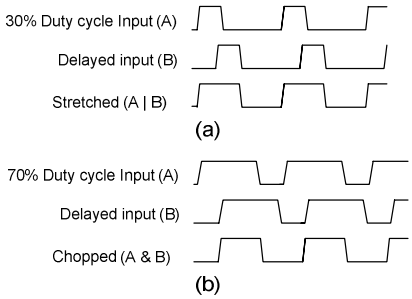

Figure 3. Timing diagram of Stretching and Chopping.

These examples also show that to correct an input signal to 50% duty cycle, the signal undergoes a maximum delay of 20% of the cycle time. This scheme is therefore less prone to power supply jitter as compared to SMD-based designs in which a signal essentially passes through a delay of 1.5 to 2 times its cycle time.

The output multiplexer selects between the stretched and chopped signal as required. It also provides a path for the original signal to the output for initial measurement. The output of this multiplexer is fed to a random sampling unit for the measurement procedure. The control unit initiates and reads the measurement to correct the output duty cycle by varying the delay setting of the programmable delay line.

A. Correction Error

The control unit uses the delay line tap that minimizes the duty cycle correction error due to the quantization effect of the minimum delay unit used in the delay line. As an example, a signal with 2ns cycle time and 30% duty cycle is required to be corrected to 50% duty cycle, and the unit delay of the delay line is 33ps. Ideally the signal should be stretched by 400ps, but the closest approximations can be achieved by selecting the 12th or 13th tap that yield 396ps and 429ps, respectively. Since the random sampling technique provides an accurate output duty cycle measurement, the control unit selects the 12th tap to keep the correction error to 4ps instead of 29ps.

B. Random Sampling Unit

Theoretically the random sampling unit is simply a gated flip-flop clocked with a random clock (See Para "C"). The practical implementation of such a sampling circuit requires careful handling of metastability issues since the clock of the latching register and the input signal may switch simultaneously. The register output could settle into an un-defined region—neither a logical high nor a logical low. Several solutions have been proposed to alleviate this problem [9],[10]. The simplest approach uses two or three cascaded flip-flops to demetastabilize the sampled value of the input signal by providing it enough time to settle down to a stable value before it is forwarded to other logic.

A simple implementation of the random sampling unit is shown in Fig. 4, which includes counters. At any transition of "Sample", "Counter 1" is loaded with "Desired Sample size (*n*)" and "Counter 2" is reset. At every edge of the random clock, "Counter 1" is decremented, and "Counter 2" is incremented when the signal is sampled as high. When "Counter 1" decrements to zero, further sampling is stopped and "Counter 2" is read to calculate the duty cycle of the input signal. The size of the counters used depends upon the required accuracy and confidence level.

Our design space exploration shows that a design with 16-bit counters could be implemented in a modest area (1700 cells of size 0.4µm x 4.8µm in 130nm technology) and provides 99% accuracy with a 99.9999% confidence. To make the correction process faster, courser measurements can be done in the beginning with smaller sized samples and more accurate measurements can be done with large sized samples towards the end of the correction process.

C. Random Clock

The ability to provide a "random clock" is a crucial factor for the proposed technique. Theoretically the random clock required for the measurement is a signal whose edge has a uniformly distributed probability of occurrence with respect to the signal to be measured, so that all parts of the measured signal can be observed with equal probability, thus making a single observation a Bernoulli trial. A practical realization of a random clock could be a signal whose source is completely un-correlated with that of the signal to be measured; thus, it could be a clock of any frequency which is not on the system to which the signal to be measured belongs. Chaos-based circuits [12] like chaotic oscillators [11],[14] can be employed to generate random numbers [13] that can be used to generate random edges.

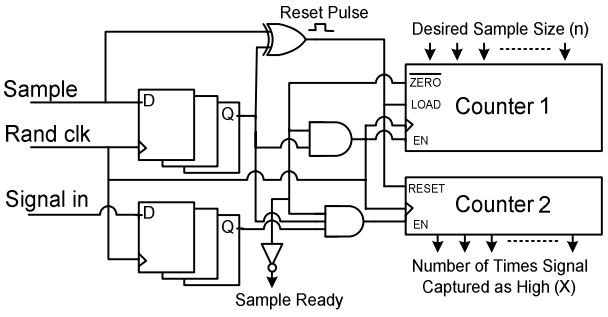

Figure 4. Implementation for random sampling unit.

The motivation for using chaotic systems to generate random numbers is that the state of a chaotic system is unpredictable, but this is true only in the long term [15]. Unpredictability means that consecutive random numbers are independent of each other in the probabilistic sense, thus providing a way of capturing the signal every time as a Bernoulli trial. The implementation of the proposed DCC does not necessarily require an on-chip random clock generator; the random clock can be injected in the circuit externally.

V. Simulation Results

Functional verification is done through post synthesis simulations of the proposed design targeted to IBM Cu-11 (130nm technology). The test bench used generates a random clock using uniformly distributed random numbers, to feed the HDL description (synthesized) of the design. For various combinations of accuracy and confidence level, the necessary sample size is found using Equation (5). An extensive series of simulation experiments were performed for different signal duty cycles and combinations of confidence level and accuracy settings, but results are shown for only 50% due to space constraints. The 50% duty cycle results were chosen because the expected error level is maximum in the measurement of 50% duty cycle signal for any given sample size and confidence level.

Fig. 5 shows the maximum observed error in 100 simulations run over each set of parameters for 50% duty cycle signal. The results are normalized to expected error for each case so that fine-level detail could be observed for all cases on the shown graph. The decreasing trend of observed error with increased confidence level is a consequence of increased sample size. It is noticeable from the results that the observed error always remained within the limits of expected error and the proposed technique is equally valid at different accuracy settings, which is favorable to design a fast converging duty cycle adjustment algorithm.

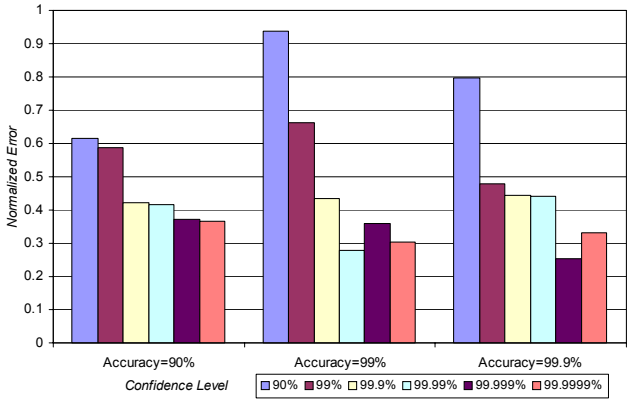

Figure 5. Maximum Observed Error Normalized by Ecpected Error

VI. Conclusion

This paper introduces a novel idea for measuring and correcting the duty cycle of on chip high speed signals or clocks that require infrequent adjustments and corrections during the regular operation of the chip. The proposed design can adjust an input signal with input duty cycle 30% to 70% to wide achievable values within the range, and cascaded multiple stages of the same circuit can achieve even wider input ranges of duty cycle. The maximum correction error of the proposed design is half the maximum delay resolution of a delay line without involving any resource-heavy analog components or custom digital components, thus making it very attractive for standard cell based ASIC designs. The theory of high-speed signal measurement using random sampling proposed in this paper can be extended for many signal manipulation and measurement applications, like relative phase measurement, multi-phase clock generation, de-skewing of parallel data lines, and clock/data alignment.

References

[1] Spiegel, Schiller, Srinivasan, “Theory and Problems of Probability and Statistics”; 2nd Edition, McGraw Hill.

[2] Kihyuk Sung; Lee-Sup Kim, “A high-resolution synchronous mirror delay using successive approximation register”, JSSC, IEEE, Volume: 39 , Issue: 11 , Nov. 2004 Pages:1997 – 2004.

[3] Kuo-Hsing Cheng et al, “A phase-locked pulse width control loop with programmable duty cycle”, Advanced System Integrated Circuits 2004. IEEE Asia-Pacific Conference.

[4] Yi-Ming Wang et al, “An all-digital 50% duty-cycle corrector”, International Symposium on Circuits and Systems 2004, Volume: 2 , 23-26 May 2004

[5] Po-Hui Yang, Jinn-Shyan Wang, “Low-voltage pulsewidth control loops for SOC applications”, JSSC, IEEE, Volume: 37 , Issue: 10 , Oct. 2002 Pages:1348 – 1351

[6] T. Gawa et al, “A 50% duty-cycle correction circuit for PLL output”, IEEE International Symposium on Circuits and Systems 2002, Volume: 4 , 26-29 May 2002.

[7] K. Nakamura, et al, ‘A CMOS 50% duty cycle repeater using complementary phase blending”, Symposium on VLSI Circuits, 2000. Digest of Technical Papers. June 2000.

[8] T.Saeki, Y. Nakaoka, M. Fujita, “A 2.5-ns clock access, 250-MHz, 256-Mb SDRAM with synchronous mirror delay”, IEEE Journal of Solid-State Circuits, Nov. 1996.

[9] J. Rabaey, “Digital Integrated Circuits”. Englewood Cliffs, NJ: Prentice- Hall, 1996.

[10] J.-N. Seizovic, “Pipeline synchronization,” Proc. IEEE ASYNC, 1994.

[11] A. J. Johansson, H. Floberg, “Random number generation by chaotic double scroll oscillator on chip; IEEE International Symposium on Circuits and Systems, 1999.

[12] G. Chen and T. Ueta, “Chaos in Circuits and Systems”, ed 2002 (Singapore: World Scientific)

[13] G.M. Bernstein, M.A. Lieberman, “Secure random number generation using chaotic circuits”, IEEE Transactions on Circuits and Systems, Volume: 37 , Issue: 9 , Sept. 1990 Pages:1157 – 1164

[14] Fengling Han et al, “n-scroll chaotic oscillators by second-order systems and double-hysteresis blocks”, Elect Ltrs, Volume: 39 , Issue: 23 , 13 Nov. 2003 Pages:1636-8

[15] B. Vizvari, G. Kolumban, “Quality evaluation of random numbers generated by chaotic sampling phase-locked loops” IEEE Transactions on Circuits and Systems, Volume: 45 , Issue: 3 , March 1998.