Programming Models and Development Software for a Space-Based Many-Core Processor

ABSTRACT
The Maestro processor is a 49-core many-core processor for space based on the TILE64 architecture and implemented in rad-hard-by-design technology by Boeing. In this paper we discuss the programming models for Maestro, the implications of the programming model on fault tolerance and flight software, and the software development tools that have been developed for Maestro. The software described here is experimental development software that allows application and algorithm evaluation on the architecture, but we believe this software can be used as the basis for flight software. The software includes libraries, performance analysis and optimization tools, and compilers. While this work was done on the Maestro chip, the principles discussed can be applied to any multi-core or many-core processor.

INDEX TERMS
• IEEE Terms
  Computer architecture, Libraries, Linux, Message passing, Programming, Real time systems, Software

• IN SPEC
  • Controlled Indexing
    aerospace computing, computer architecture, microprocessor chips, multiprocessing systems, program compilers, program processors, software architecture, software fault tolerance, software libraries, software performance evaluation
  • Non Controlled Indexing
    49-core manycore processor, Maestro chip, Maestro processor, TILE64 architecture, fault tolerance, flight software, multicore processor, optimization tool, programming model, rad-hard-by-design technology, software compiler, software development tool, software library, space-based manycore processor

• Author Keywords
  Multi-core programming, parallel software, space-based processing