I  Design

Goal of this project is to understand the concept of structural modules as well as getting familiar with the CAD tools. You may choose to use VHDL and/or schematics to do this project on Xilinx ISE and ModelSim.

II  Simulation

Write the VHDL code and/or draw schematic of the design in Xilinx ISE project. When the design is complete, compile, debug, and simulate the design using ModelSim. Write test vectors of various inputs to test the correctness of the design functionalities. Generate waveform for the simulation.

III  Write-Up

Write a description of the design explaining your methodology and specification of the design. Include the print outs of the VHDL source code and/or schematics of the design. Also print out the waveform of the simulation that verifies the ALU functionality.

IV  Extra Credit

Map the design using a particular FPGA device. Find the estimated critical path timing. Add pipeline registers in within the logic to shorten the critical path.